Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20210006	04-Mar.-2021	New issue	Hank Lin

■ Product Description

The CS26LV81923A is a high performance, high speed, low power pseudo SRAM organized as 5,243,788 words by 16 bits and operates from a wide range of 2.7 to 3.3V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and low power features with a typical standby current of 30uA and maximum access time of 70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.
The CS26LV81923 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS26LV81923 is available 48-balls TFBGA-6x8mm package.

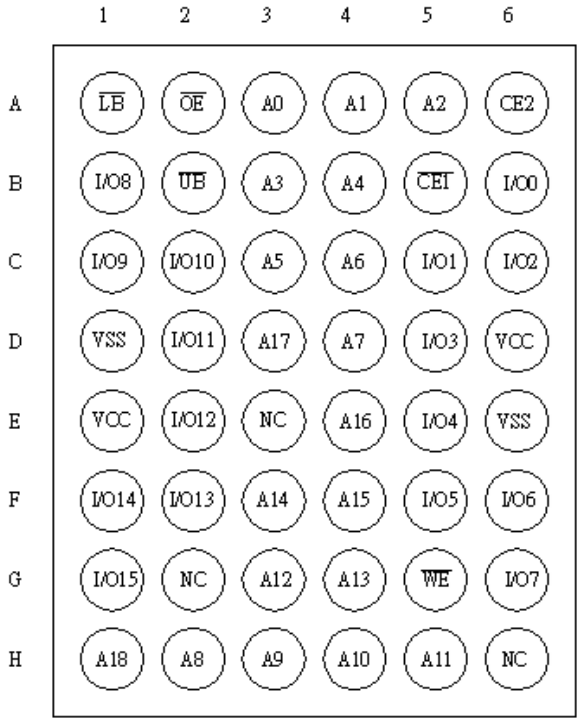
■ Features

- Low operation voltage : 2.7 ~ 3.3V
- Ultra low power consumption :
  Vcc = 3.0V, 3mA@1MHz (Max.) operating current
  30uA (Typ.) CMOS standby current
- High speed access time : 70ns at Vcc = 3.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible,
- Asynchronous SRAM compatible operation
- Easy expansion with /CE and /OE options.

■ Product Family

Part No.	Operating Temp	Vcc. Range (V)	Speed (ns)	Standby (Typ.)	Package Type
CS26LV81923A	0~70°C	2.7~3.3	70	30 uA (Vcc = 3.0V)	Dice
					48 Balls TFBGA-6x8mm
	-40~85°C	2.7~3.3	70	30 uA (Vcc = 3.0V)	Dice
					48 balls TFBGA-6x8mm

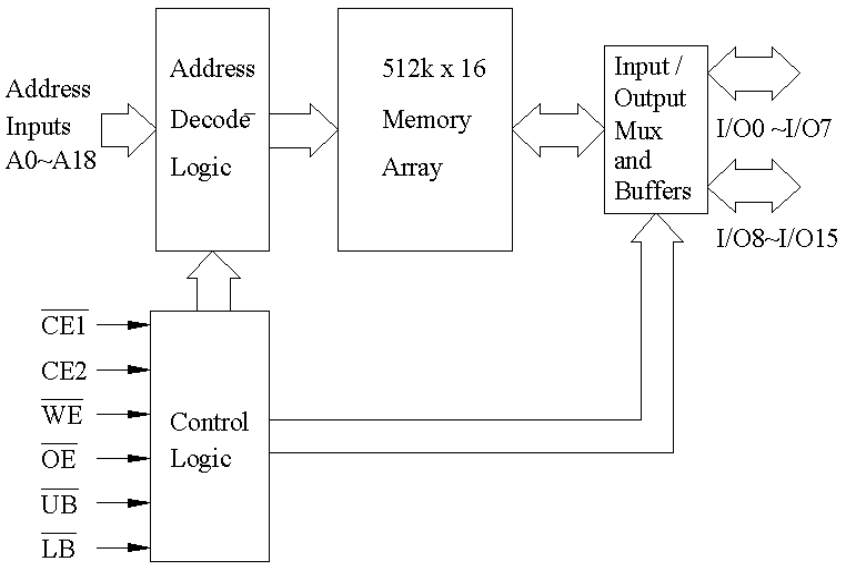
■ Pin Configuration



48 balls TFBGA-6x8mm

(Top View)

■ Functional Block Diagram



■ Pin Description

Name	Type	Function
A0-A18	input	address inputs
/CE1 & CE2	input	/CE is active LOW. Chip enables must be active when data read from or write to the device. if chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
/WE	input	The write enable input is active LOW and controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins; when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB & /UB	input	Lower byte and upper byte data input/output control pins.
I/O0 ~ I/O15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Vss	Power	Ground

■ Truth Table

MODE	/CE1	CE2	/WE	/OE	/LB	/UB	IO0~7	IO8~15	Vcc Current
Not Selected	H	X	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
					H	L	High Z	D_{OUT}	I_{CC}
					L	H	D_{OUT}	High Z	I_{CC}
Write	L	H	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
					H	L	X	D_{IN}	I_{CC}
					L	H	D_{IN}	X	I_{CC}

■ Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.2 to Vcc+0.3	V
T_{BIAS}	Temperature Under Bias	-40 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ DC Electrical Characteristics (T_A = 0 to + 70°C , V_{CC} = V_{CCQ} = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{IL}	Input Low Voltage (2)		-0.2		$0.2V_{CCQ}$	V
V_{IH}	Input High Voltage (2)		$0.8V_{CCQ}$		V_{CC}+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA			$0.2V_{CCQ}$	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	$0.8V_{CCQ}$			V
I_{CC}	Operating Power Supply Current	/CE1≦V_{IL}, CE2≧V_{IH} I_{DQ}=0mA, F=F_{MAX}(3)			25	mA
I_{CCSB}	Standby Supply - TTL	/CE1&CE2≧V_{IH}, Other Inputs≧V_{IH} or≦V_{IL}			0.3	mA
I_{CCSB1}	Standby Current -CMOS	/CE1&CE2≧V_{CC}-0.2V & V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V			70	uA

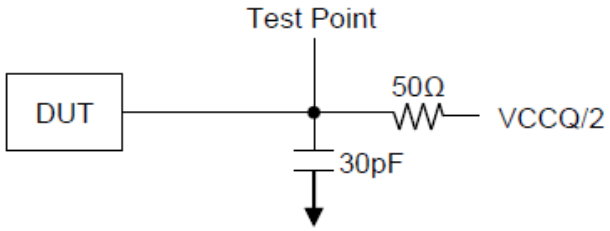
1. Typical characteristics are at T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$.

■ Capacitance (1) (T_A = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not tested.

■ AC Test Conditions



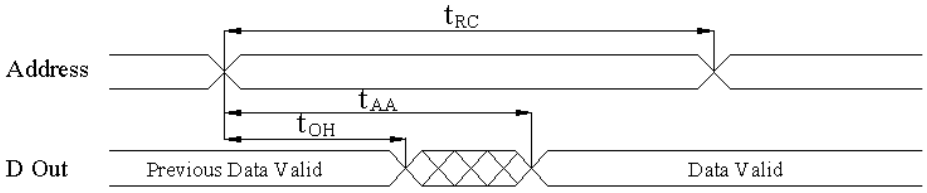
■ AC Characteristics

Read cycle

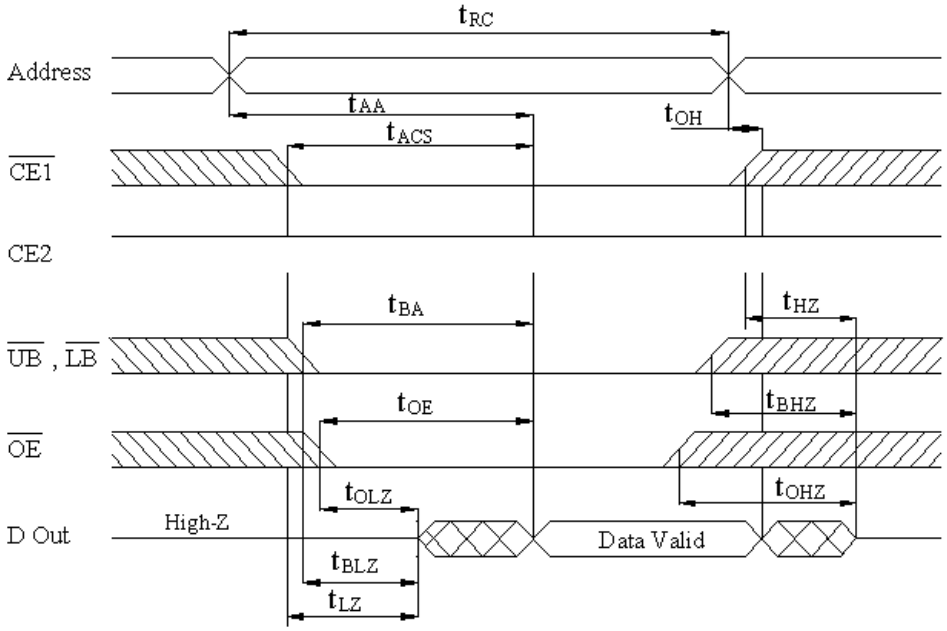
Parameter Name	Name	Min	Max	Unit
Read cycle time	t_{RC}	70	20k	ns
Address access time	t_{AA}	-	70	ns
Chip enable access time (/CE1)	t_{ACS}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	70	ns
Output hold from address change	t_{OH}	5	-	ns
Chip enable to output in low Z (/CE1)	t_{LZ*}	10	-	ns
Output enable to output in low Z (/OE)	t_{OLZ*}	5	-	ns
Byte enable to output in low Z	t_{BLZ*}	10	-	ns
Chip disable to output in High Z (/CE1)	t_{HZ*}	0	5	ns
Output disable to output in High Z (OE)	t_{OHZ*}	0	5	ns
Byte disable to output in High Z	t_{BHZ*}	0	5	ns
/CE1 High Pulse Width	t_{CP}	10	-	ns

*These parameters are sampled and are not 100% tested

Read Cycle 1- (/CE1=/OE=V_{IL}, /WE= CE2=V_{IH})



Read Cycle 2 – (/WE=V_{IH})



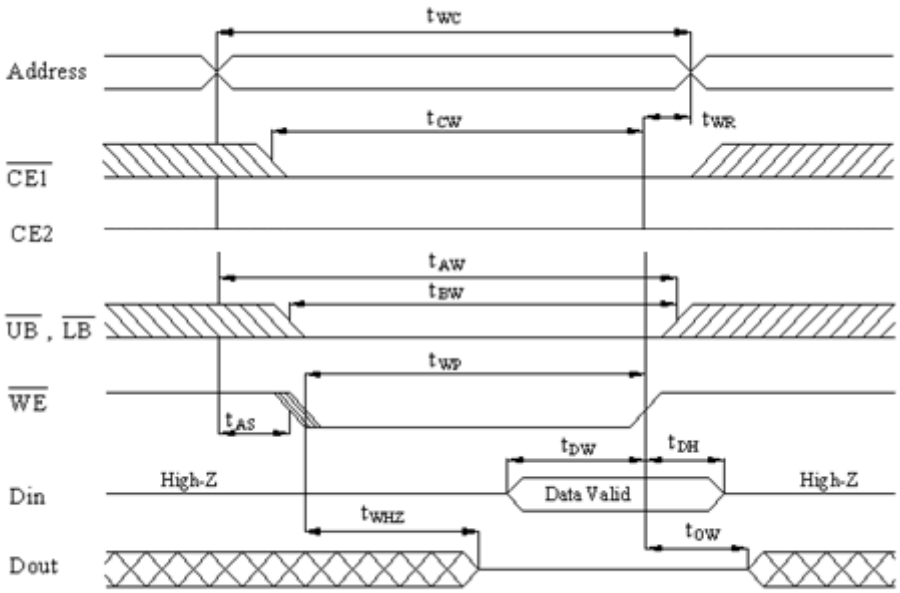
Write Cycle

Parameter Name	Name	Min	Max	Unit
Write cycle time	t_{WC}	70	20K	ns
Byte enable to end of write	t_{BW}	60	-	ns
Address valid to end of write	t_{AW}	60	-	ns
Chip select to end of write	t_{CW}	60	-	ns
Data set up time	t_{DW}	20	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns

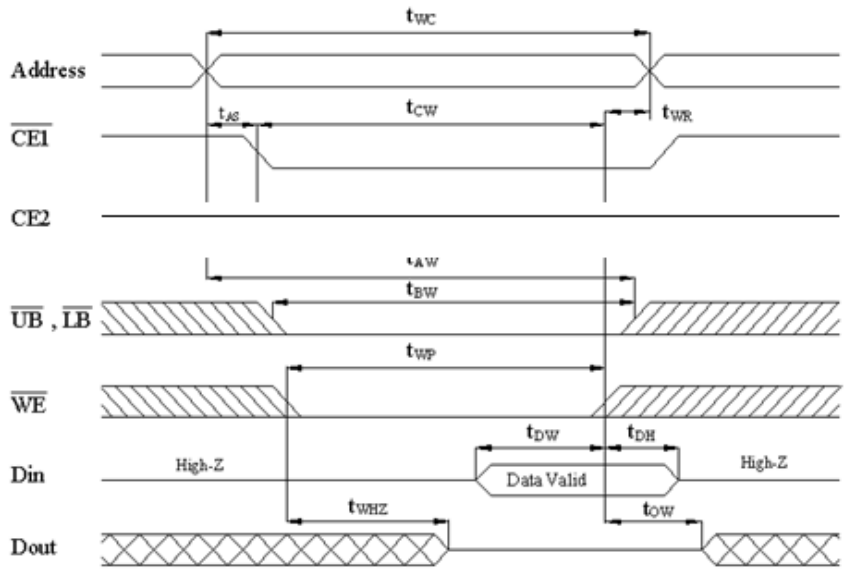
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OW*}	5	-	ns
Write to output high Z	t_{WHZ*}	-	5	ns
/CE1 High Pulse Width	t_{CP}	10	-	ns

*These parameters are sampled and are not 100% tested

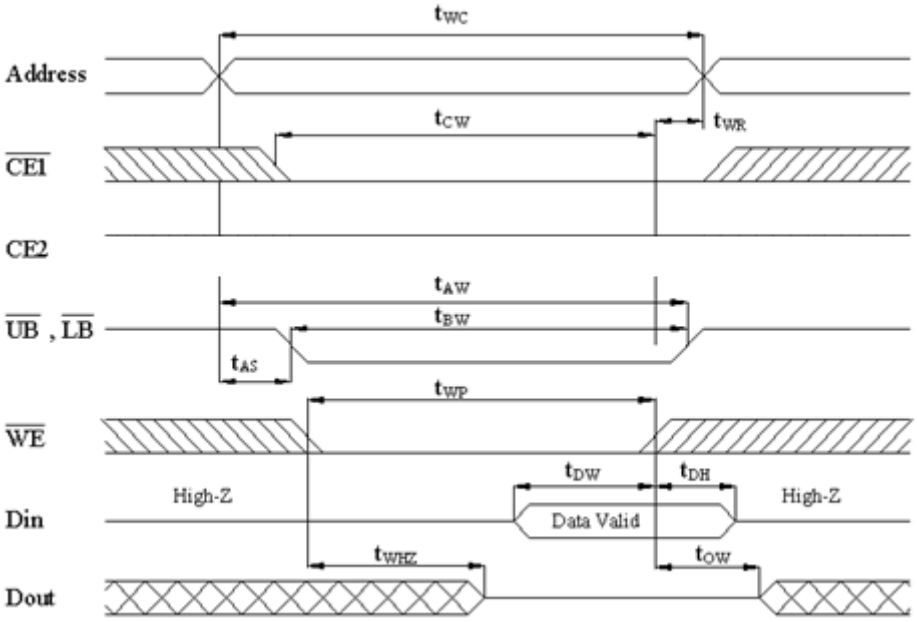
Write Cycle 1- (/WE controlled)



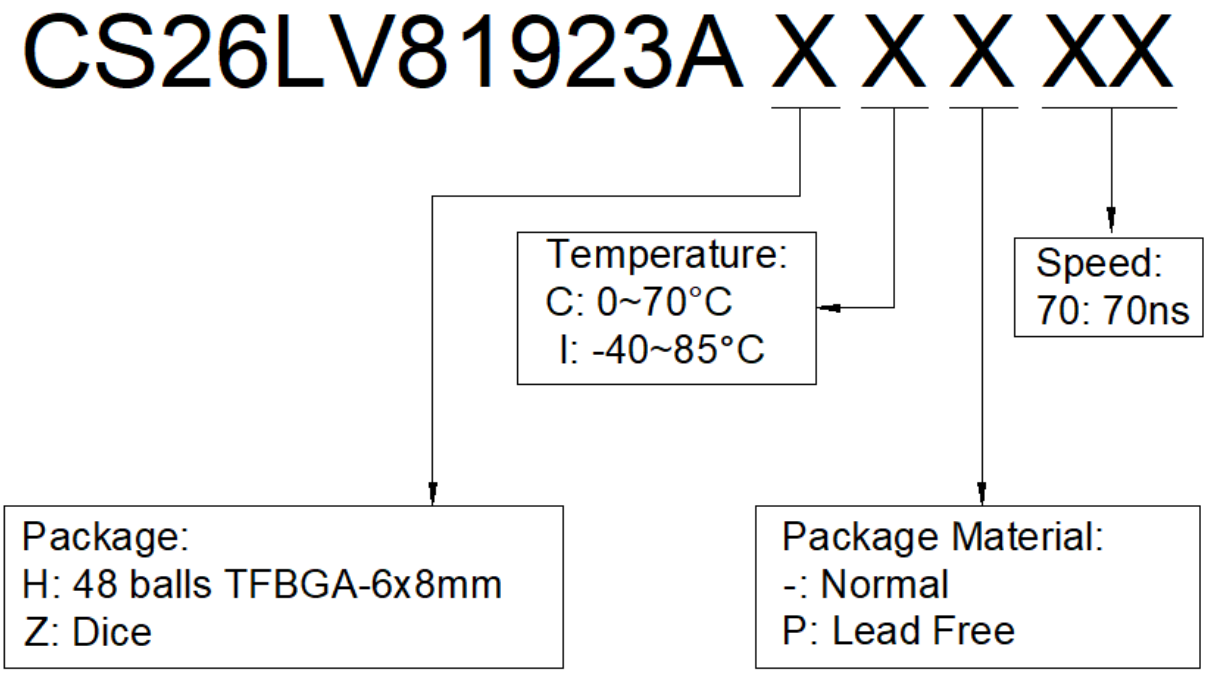
Write Cycle 2- (/CE1 controlled)



Write Cycle 3- (/UB, /LB controlled)

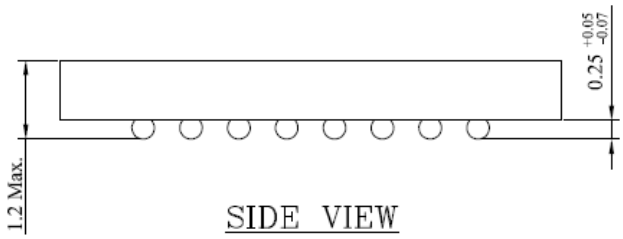


■ Order information



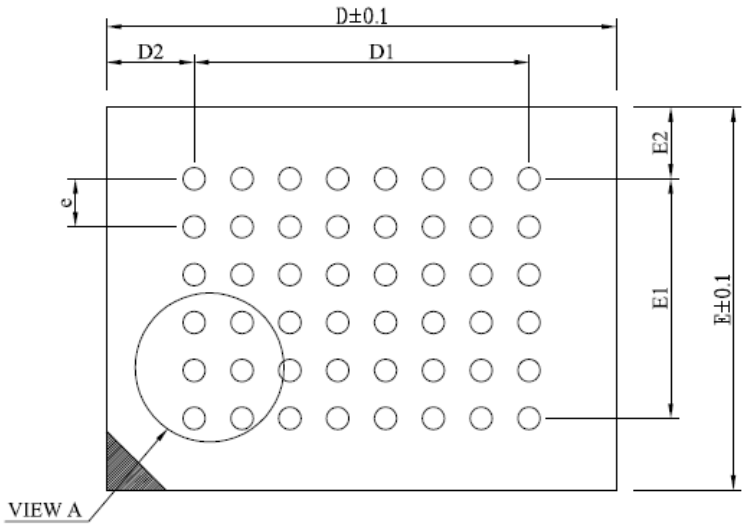
■ Package Outline

48 balls TFBGA-6x8mm

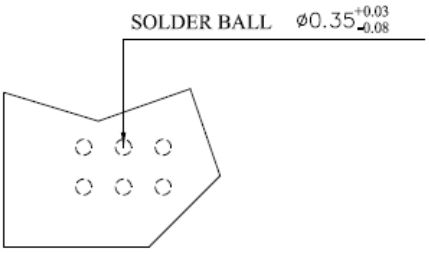


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025