



# High Speed Super Low Power SRAM

512K Word By 8 Bit

CS18LV41963

## Cover Sheet and Revision Status

版別 (Rev.)	DCC No.	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20160057	Jul. 12, 2016	New issue	Hank Lin
2.0	20170013	Jun. 22, 2017	Revise 32L STSOP(I)-8x13.4mm package outline	Hank Lin
3.0	20200019	Dec. 29, 2020	Revise ICC (operating current) 45ns- 20mA, 55ns- 20mA, 70ns- 15mA	Hank Lin
4.0	20230006	Mar. 21, 2023	Revise I <sub>CCDR</sub> (TYP. & MAX) from ( 0.3uA & 2uA) to (2uA & 6uA)	Hank Lin



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## GENERAL DESCRIPTION

The CS18LV41963 is a high performance, high speed, and super low power CMOS Static Random Access Memory organized as 524,288 words by 8 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.50uA and maximum access time of 45/55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS18LV41963 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV41963 is available in JEDEC standard 32-pin sTSSOP 1 -8x13.4 mm, TSOP 1 -8x20mm, TSOP 2 -400mil and SOP -450 mil packages.

## FEATURES

- Low operation voltage: 2.7 ~ 3.6V
- Ultra low power consumption :
  - operating current: 20mA (Max.) @ $t_{AA}=45ns$
  - standby current : 2uA (Typ.)
- Fast access time: 45/55/70ns (Max.)
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.

## Product Family

Product Family	Operating Temp	Standby (Max.) (V <sub>cc</sub> = 3.6V)	V <sub>cc</sub> . Range (V)	Speed (ns)	Package Type
CS18LV41963	0~70°C	8 uA	2.7~3.6	45/55/70	32L SOP
	-40~85°C				32L STSOP 1
					32L TSOP 1
					32L TSOP 2
					Dice

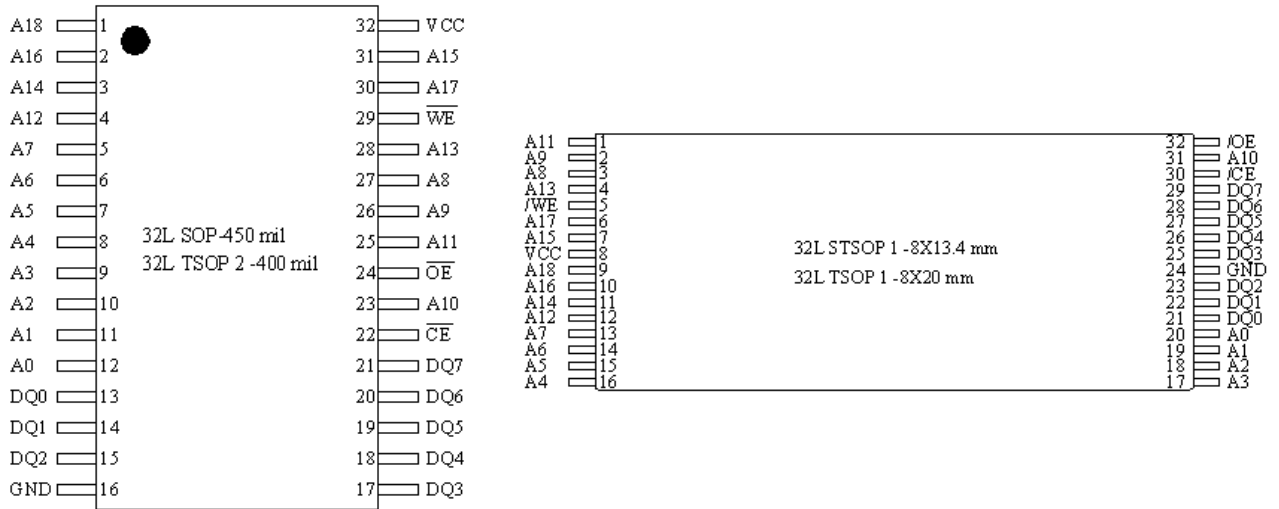


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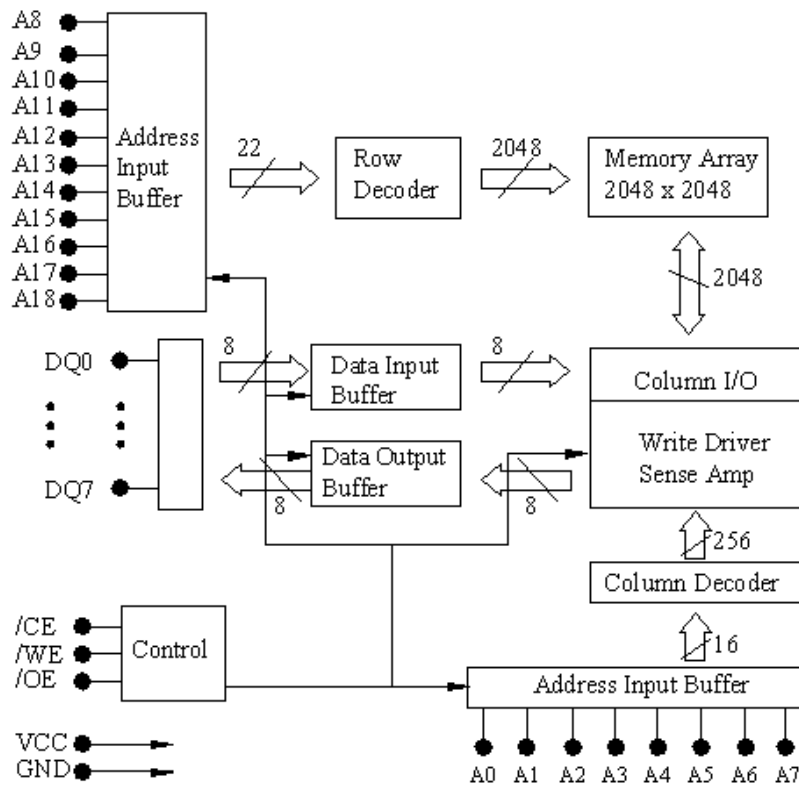
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## PIN CONFIGURATIONS



## FUNCTIONAL BLOCK DIAGRAM





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## PIN DESCRIPTIONS

Name	Type	Function
A0 – A18	Input	Address inputs for selecting one of the 524,288 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
V <sub>CC</sub>	Power	Power Supply
Gnd	Power	Ground
NC		No connection

## TRUTH TABLE

MODE	/CE	/WE	/OE	DQ0~7	V <sub>CC</sub> Current
Standby	H	X	X	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	High Z	I <sub>CC</sub>
Read	L	H	L	D <sub>OUT</sub>	I <sub>CC</sub>
Write	L	L	X	D <sub>IN</sub>	I <sub>CC</sub>



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## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>BIAS</sub>	Temperature Under Bias	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

## CAPACITANCE <sup>(1)</sup> (T<sub>A</sub> = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	6	pF
C <sub>DQ</sub>	Input/output Capacitance	V <sub>I/O</sub> =0V	8	pF

*This parameter is guaranteed and not tested.*



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## DC ELECTRICAL CHARACTERISTICS ( $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ )

Parameter Name	Parameter	Test Conduction	MIN	TYP <sup>(1)</sup>	MAX	Unit
$V_{IL}$	Guaranteed Input Low Voltage <sup>(3)</sup>	$V_{CC}=3\text{V}$	-0.3		0.8	V
$V_{IH}$	Guaranteed Input High Voltage <sup>(2)</sup>	$V_{CC}=3\text{V}$	2.2		$V_{CC}+0.2$	V
$I_{IL}$	Input Leakage Current	$V_{CC}=\text{MAX}$ , $V_{IN}=0$ to $V_{CC}$	-1		1	$\mu\text{A}$
$I_{OL}$	Output Leakage Current	$V_{CC}=\text{MAX}$ , $/\text{CE}=V_{IN}$ , or $/\text{OE}=V_{IN}$ , $V_{IO}=0\text{V}$ to $V_{CC}$	-1		1	$\mu\text{A}$
$V_{OL}$	Output Low Voltage	$V_{CC}=\text{MAX}$ , $I_{OL} = 2\text{mA}$			0.4	V
$V_{OH}$	Output High Voltage	$V_{CC}=\text{MIN}$ , $I_{OH} = -1\text{mA}$	2.4			V
$I_{CC}$	Operating Power Supply Current	$/\text{CE}=V_{IL}$ , $I_{DQ}=0\text{mA}$ , $F=F_{\text{MAX}}^{(3)}$	45ns		20	mA
			55ns		20	
			70ns		15	
$I_{CCSB}$	Standby Supply - TTL	$/\text{CE}=V_{IH}$ , $I_{DQ}=0\text{mA}$ ,			0.3	mA
$I_{CCSB1}$	Standby Current -CMOS	$/\text{CE}\geq V_{CC}-0.2\text{V}$ , $V_{IN}\geq V_{CC}-0.2\text{V}$ or $V_{IN}\leq 0.2\text{V}$		2	6	$\mu\text{A}$

1. Typical characteristics are at  $T_A = 25\text{ }^{\circ}\text{C}$ .
2. Overshoot :  $V_{CC} + 2.0\text{V}$  in case of pulse width  $\leq 20\text{ns}$ .
3. Undershoot :  $- 2.0\text{V}$  in case of pulse width  $\leq 20\text{ns}$ .
4. Overshoot and undershoot are sampled, not 100% tested.



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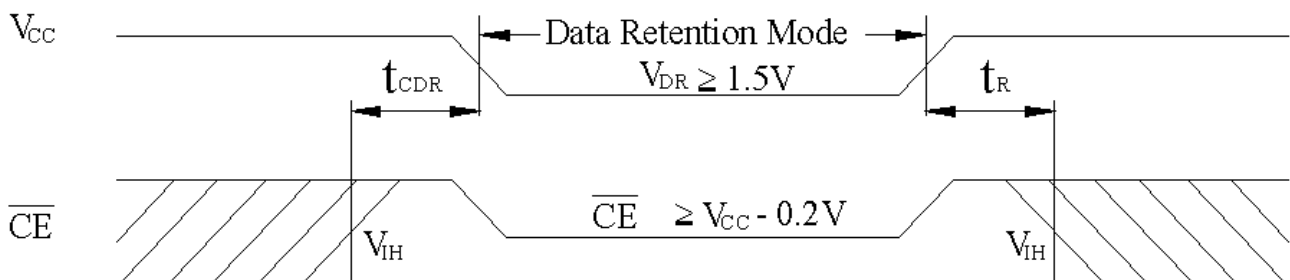
CS18LV41963

## DATA RETENTION CHARACTERISTICS (T<sub>A</sub> = 0°C to + 70°C)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Data Retention	$V_{CE} \geq V_{CC} - 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	1.5			V
I <sub>CCDR</sub>	Data Retention Current	$V_{CE} \geq V_{CC} - 0.2V, V_{CC} = 1.5V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		2	6	uA
T <sub>CDR</sub>	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t <sub>R</sub>	Operation Recovery Time		t <sub>RC</sub> (1)			ns

1. Read Cycle Time.

## LOW V<sub>CC</sub> DATA RETENTION WAVEFORM (/CE Controlled)

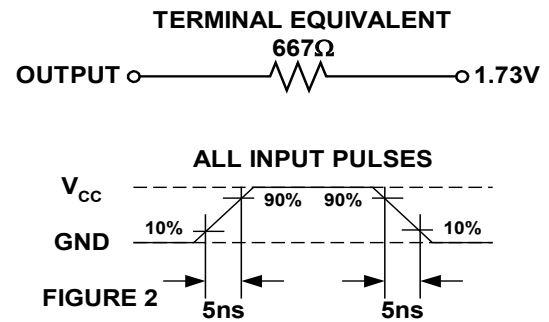
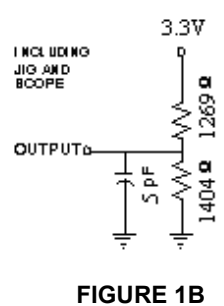
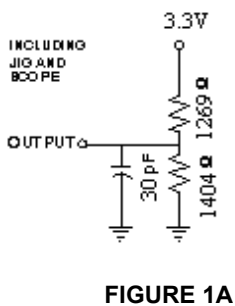




### AC TEST CONDITIONS    KEY TO SWITCHING WAVEFORMS

Input Pulse Levels	$V_{cc}/0V$	WAVEFORMS	INPUTS	OUTPUTS
Input Rise and Fall Times	3ns		MUST BE STEADY	MUST BE STEADY
Input and Output Timing Reference Level	$0.5V_{cc}$		MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
Output Load	See FIGURE 1A and 1B		MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
			DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
			DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

### AC TEST LOADS AND WAVEFORMS





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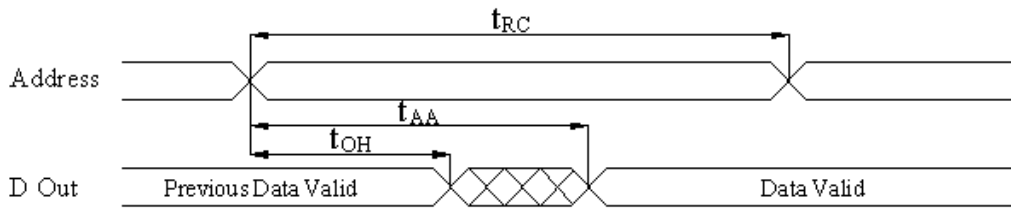
## AC ELECTRICAL CHARACTERISTICS ( $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ )

### < READ CYCLE >

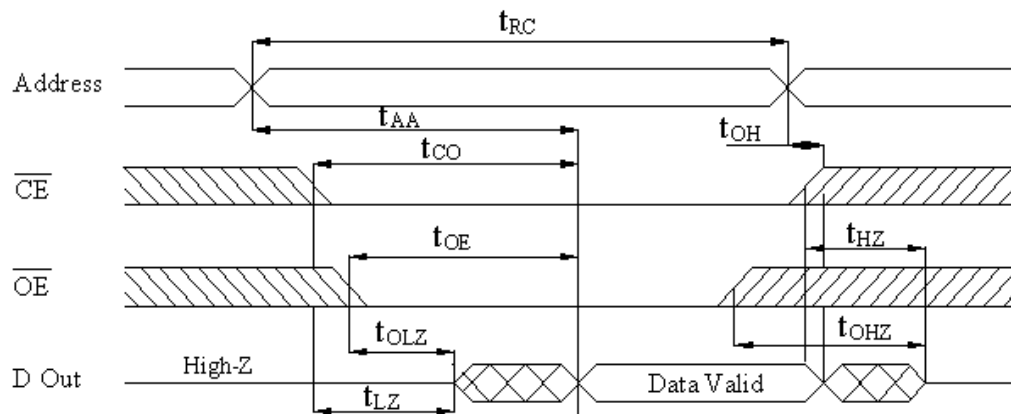
JEDEC Parameter Name	Parameter Name	Description	45ns		55ns		70ns		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
tAVAX	tRC	Read Cycle Time	45		55		70		ns
tAVQV	tAA	Address Access Time		45		55		70	ns
tELQV	tCO	Chip Select Access Time (/CE)		45		55		70	ns
tGLQV	tOE	Output Enable to Output Valid		22		25		35	ns
tELQX	tLZ	Chip Select to Output Low Z (/CE)	10		10		10		ns
tGLQX	tOLZ	Output Enable to Output in Low Z	5		5		5		ns
tEHQZ	tCHZ	Chip Deselect to Output in High Z (/CE)		18		20		25	ns
tGHQZ	tOHZ	Output Disable to Output in High Z		18		20		25	ns
tAXOX	tOH	Out Disable to Address Change	10		10		10		ns

### SWITCHING WAVEFORMS (READ CYCLE)

#### READ CYCLE 1.



#### READ CYCLE 2.



**NOTES:**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}$  (Max.) is less than  $t_{LZ}$  (Min.) both for a given device and from device to device interconnection.



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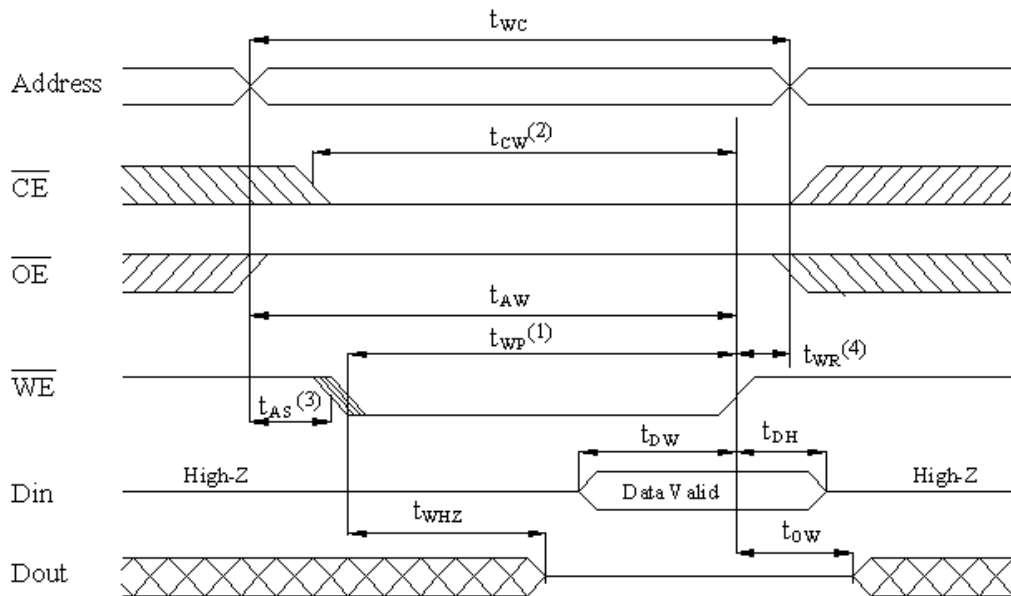
## AC ELECTRICAL CHARACTERISTICS ( $T_A = 0\text{ }^{\circ}\text{C}$ to $+70\text{ }^{\circ}\text{C}$ , $V_{CC} = 3.0\text{V}$ )

### < WRITE CYCLE >

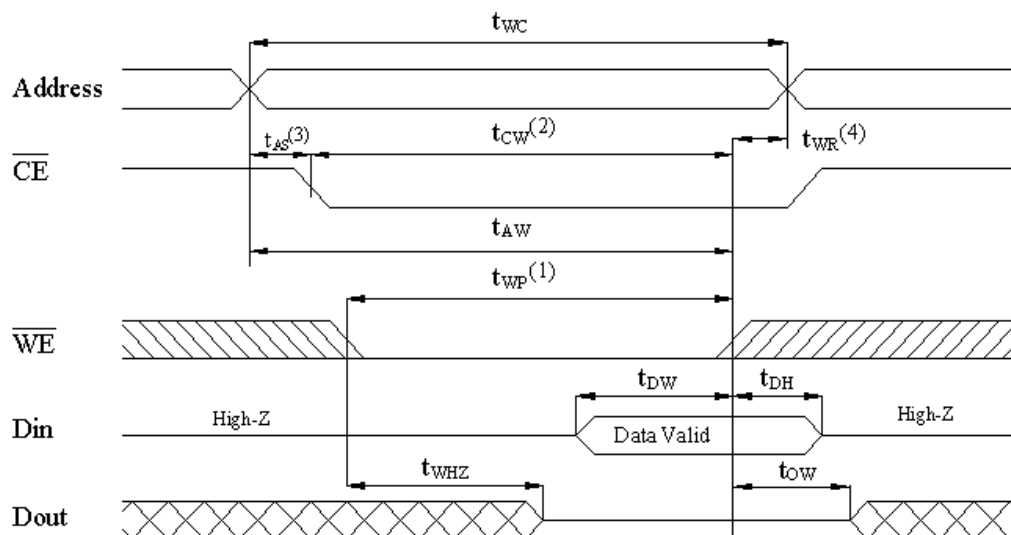
JEDEC Parameter Name	Parameter Name	Description	45ns		55ns		70ns		Unit
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	45		55		70		ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write	35		45		60		ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0		0		0		ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	35		45		60		ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	35		40		55		ns
$t_{WHAX}$	$t_{WR}$	Write Recovery Time (/CE, /WE)	0		0		0		ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z		18		20		25	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	25		25		30		ns
$t_{WHDX}$	$t_{DH}$	Data Hold from Write Time	0		0		0		ns
$t_{WHOX}$	$t_{OW}$	End of Write to Output Active	5		5		5		ns

### SWITCHING WAVEFORMS (WRITE CYCLE)

#### WRITE CYCLE 1. (/WE Controlled)



#### WRITE CYCLE 2. (/CE1 Controlled)



NOTES:

1. A write occurs during the overlap ( $t_{WP}$ ) of low  $\overline{CE}$  and low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CE}$  goes low. A write ends at the earliest transition when  $\overline{CE}$  goes high and  $\overline{WE}$  goes high. The  $t_{WP}$  is measured from the beginning of the write to the end



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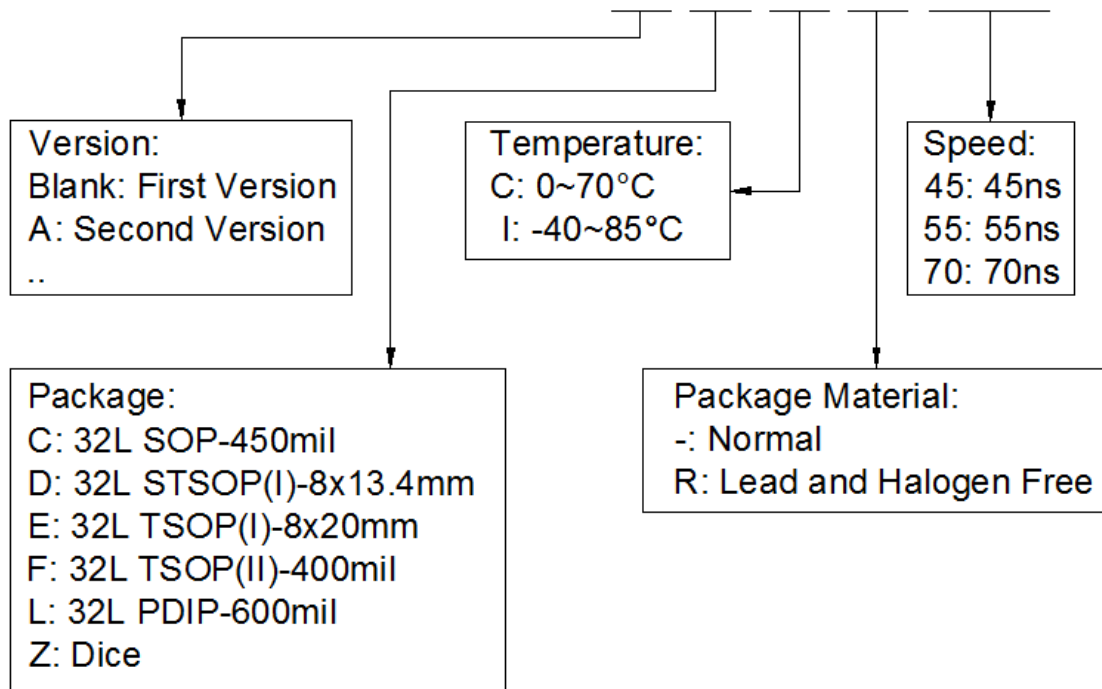
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of write.

2.  $t_{CW}$  is measured from the /CE going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change. TWR applied in case a write ends as /CE or /WE going high.

## ORDER INFORMATION

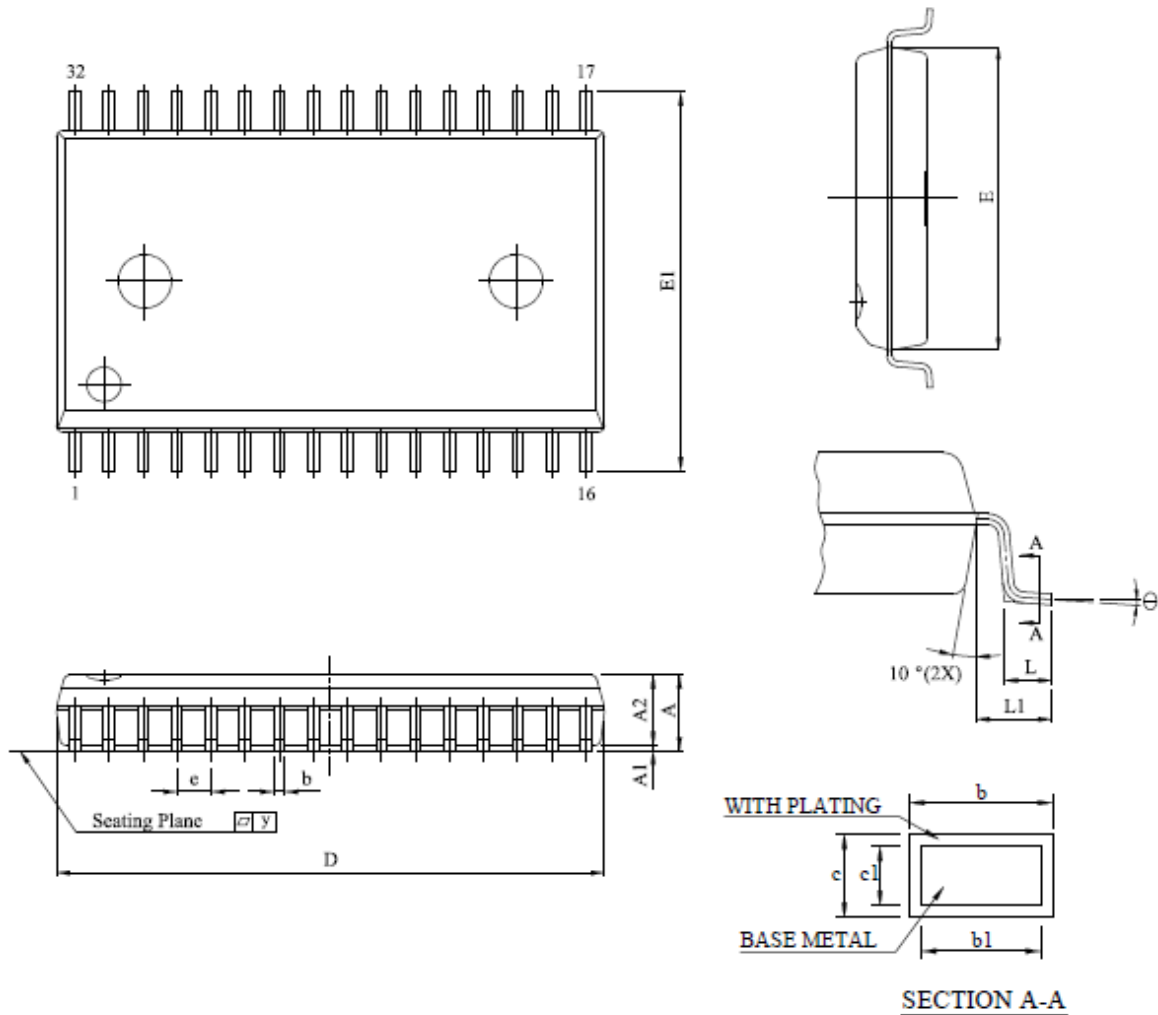
CS18LV41963 X X X X XX



Note: Package material code "R" meets ROHS

### PACKAGE OUTLINE

#### 32L SOP-450mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	⊙
UNIT																
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	-	0°
	Nom.	2.821	0.229	2.680	-	-	-	-	20.447	11.303	14.097	1.270	0.834	1.397	-	-
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	-	0°
	Nom.	0.111	0.009	0.1055	-	-	-	-	0.805	0.445	0.555	0.050	0.033	0.055	-	-
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

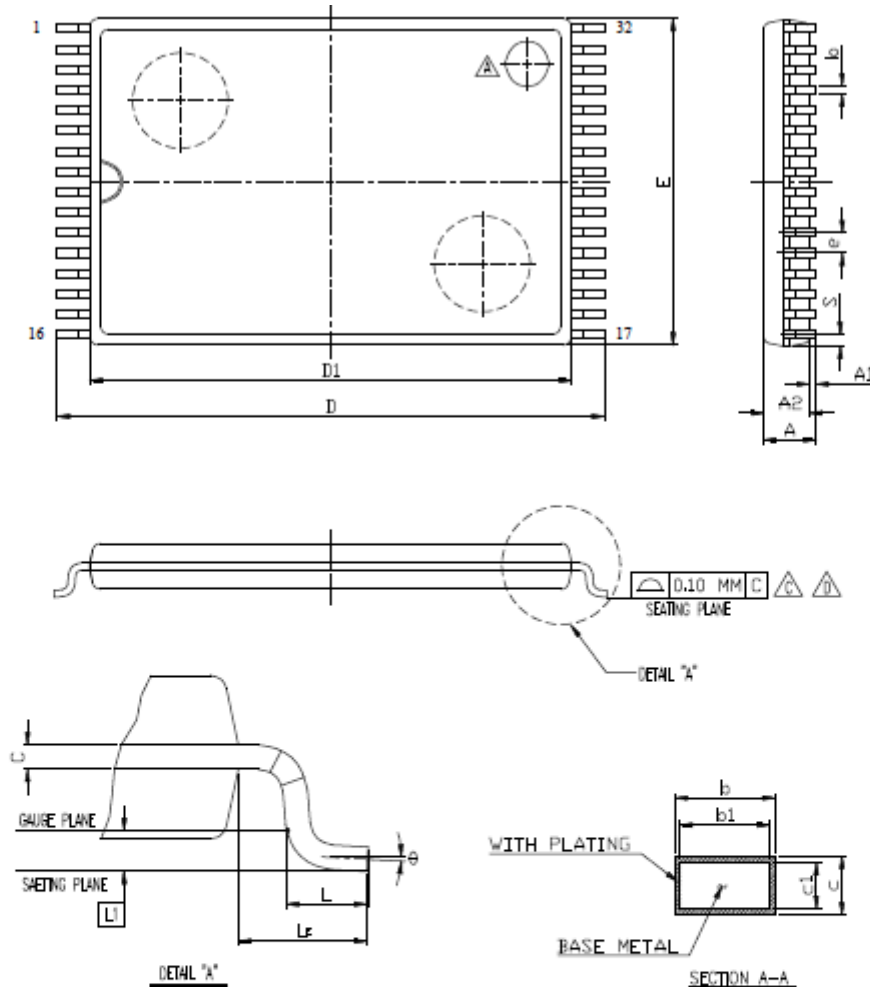


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32L STSOP (I)-8x13.4mm

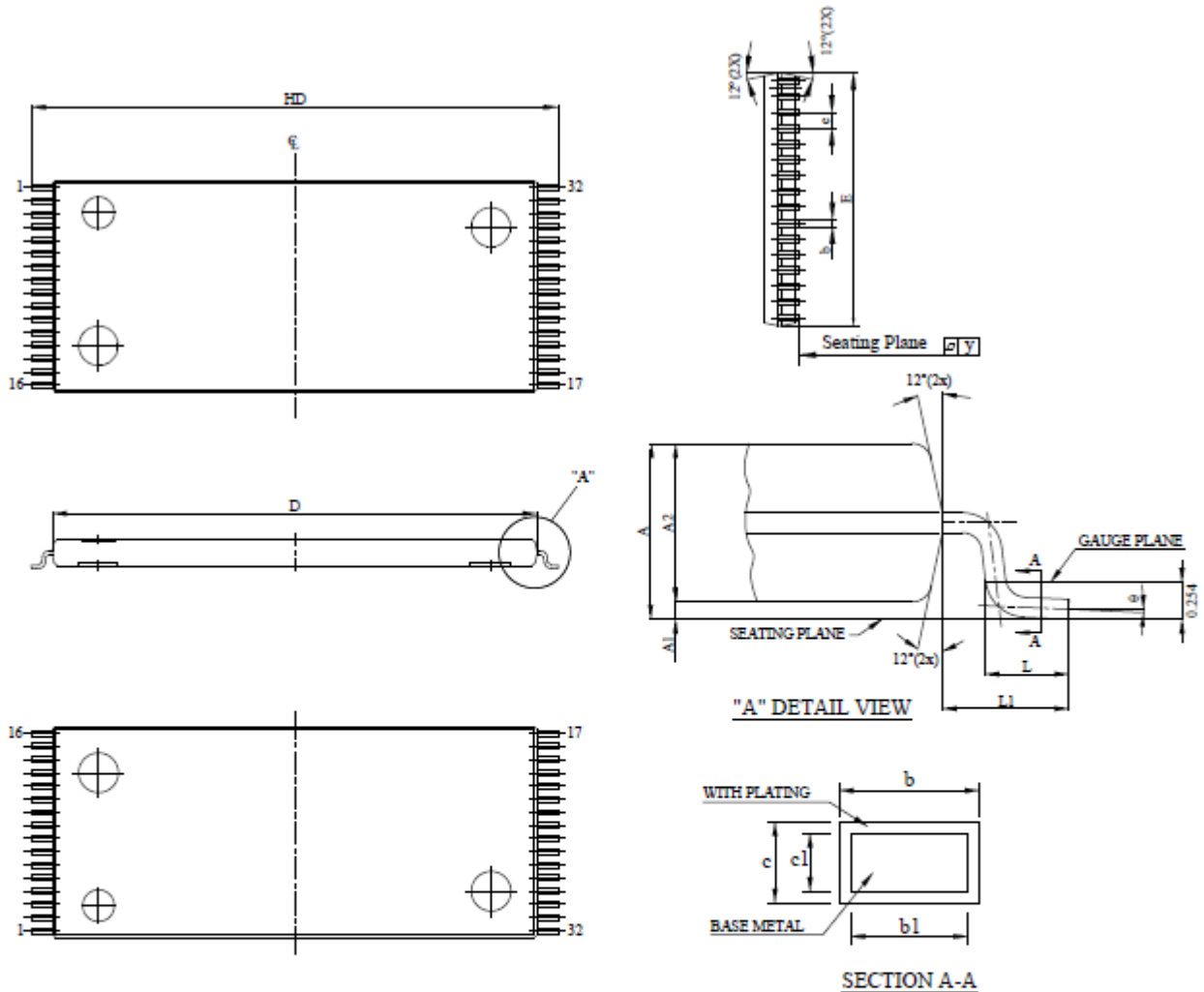


Note: Dimensions D1 and E do not include mold protrusions.  
D1 and E are maximum plastic body size dimensions including mold mismatch.

SYMBOL	A	A1	A2	b	b1	c	c1	E	e	D	D1	L	L1	LE	S	e
mm	Min.		0.90	0.17	0.17	0.10	0.10	7.90	0.50 TYP.	13.20	11.70	0.30	0.25 BSC	0.675	0.278 TYP.	0
	Nom.		1.00	0.22	0.20	-	-	8.00		13.40	11.80	0.50		0.278		3
	Max.	1.20		1.05	0.27	0.23	0.21	0.16		8.10	13.60	11.90		0.70		0.278
inch	Min.		0.035	0.007	0.007	0.004	0.004	0.311	0.020 TYP.	0.520	0.461	0.012	0.010 BSC	0.027	0.0109 TYP.	0
	Nom.		0.039	0.009	0.008	-	-	0.315		0.528	0.465	0.020		0.0109		3
	Max.	0.047		0.041	0.011	0.009	0.008	0.006		0.319	0.535	0.469		0.028		0.0109



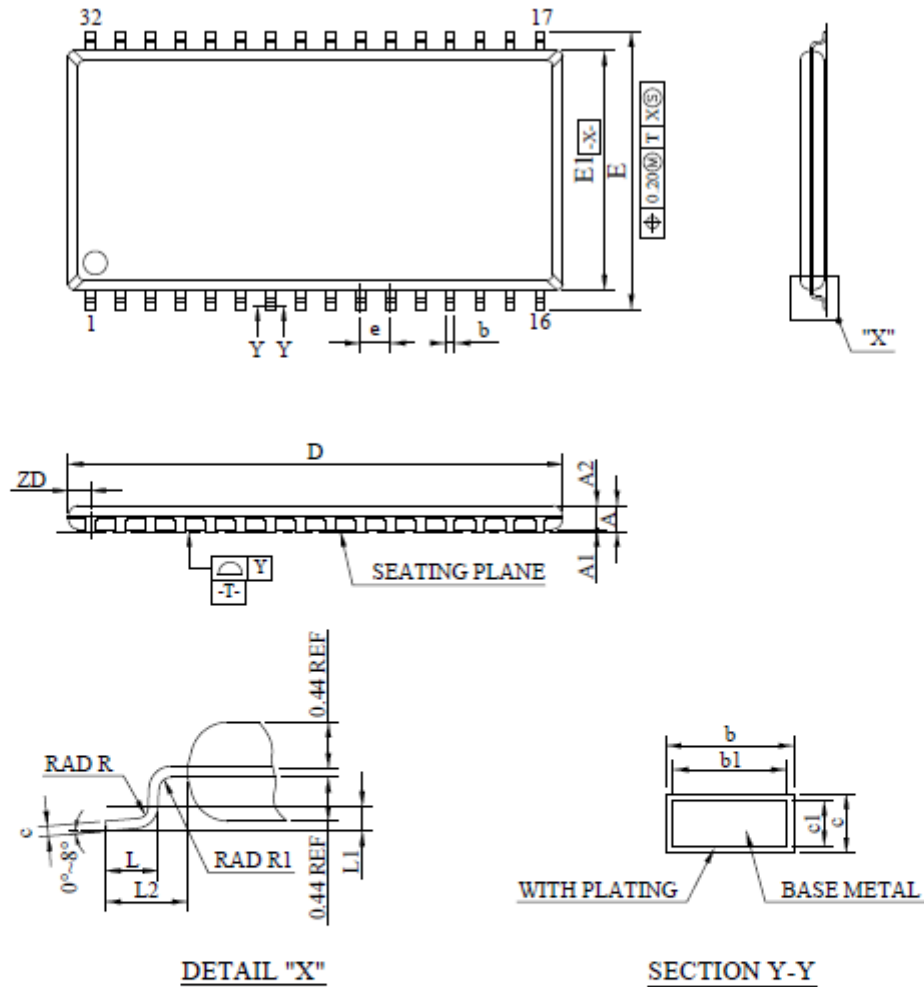
### 32L TSOP (I)-8x20mm



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	⊙
UNIT																
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	-	-	18.40	8.00	0.50	20.00	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	-	-	0.724	0.315	0.020	0.787	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

### 32L TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y			
UNIT																						
mm	Min.	-	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03	1.27 bsc	0.40	0.25 bsc	0.8 ref	0.12	0.12	0.95 ref	-			
	Nom.	-	0.10	1.00	-	0.40	-	0.127	20.95	11.76	10.16		0.50			-	-		-	-	-	-
	Max.	1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29		0.60			0.25	-		-	0.10		
inch	Min.	-	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394	0.050 bsc	0.016	0.010 bsc	0.031 ref	0.005	0.005	0.037 ref	-			
	Nom.	-	0.004	0.039	-	0.016	-	0.005	0.825	0.463	0.400		0.020			-	-		-	-	-	
	Max.	0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405		0.024			0.010	-		0.004			