Revision History

Rev. No.	History	Issue Date	Remark
1.0	New issue (65nm process)	May. 27, 2015	
2.0	Add test conditions in AC Characteristics	Sep. 06, 2016	

Product Description

The CS26LV16163C is a high performance, high speed, low power pseudo SRAM organized as 1M words by 16 bits and operates from a wide range of 2.6 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and maximum access time of 70ns in 3.3V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS26LV16163C has the page access operation, page size is 16 words, and has a deep power down feature, reducing the power consumption significantly when chip is deselected.

The CS26LV16163C is available 48-ball TFBGA package.

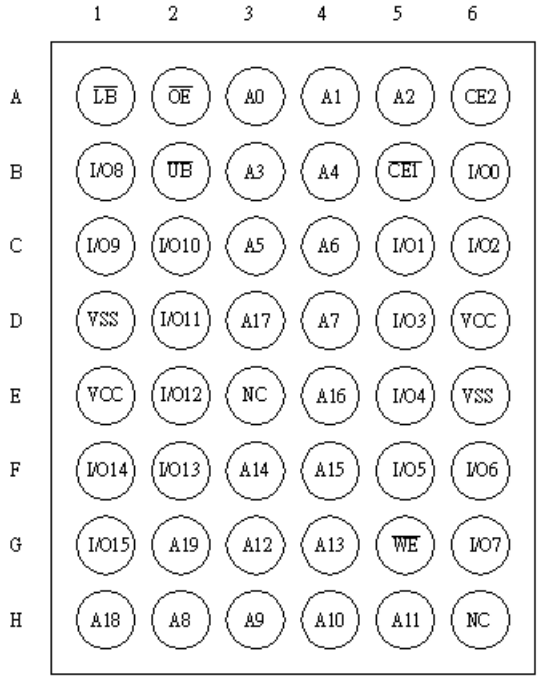
Features

- Single power supply voltage of 2.6 to 3.6V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 120 uA(Max)
  - Deep power-down standby 20 uA (Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 25ns
  - Page Access Time: 25ns

Product Family

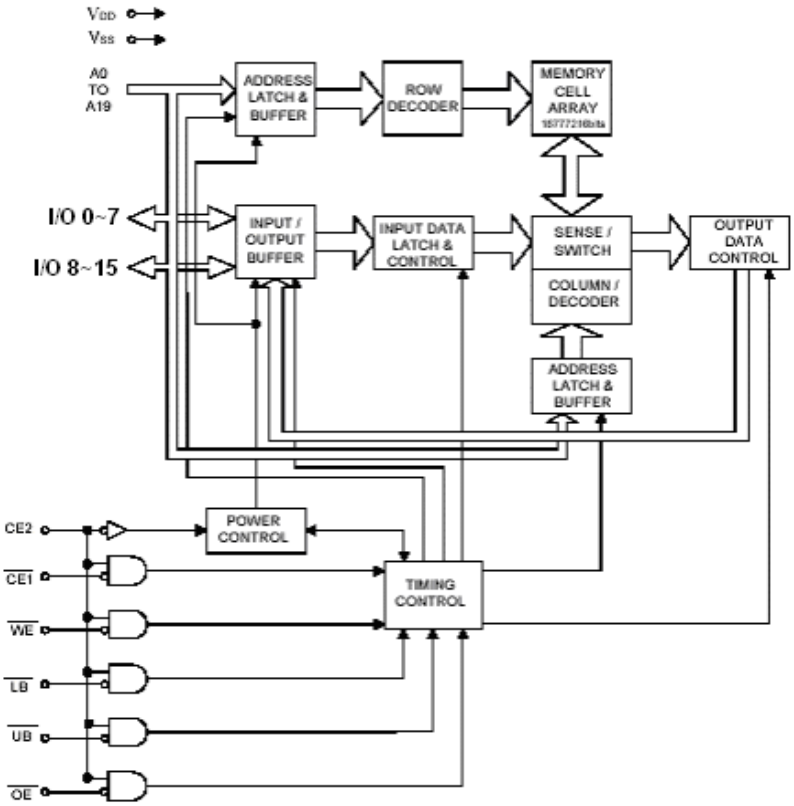
Part No.	Operating Temp	V_{CC} Range	Speed	Standby (ISB, Max.)	Package Type
CS26LV16163C	0~70 °C	2.6~3.6V	70ns	120uA	Dice 48 TFBGA-6x8mm
	-40~85 °C			120uA	

Pin Configuration



48 Ball TFBGA-6x8mm Top View

Functional Block Diagram



Pin Description

Name	Type	Function
A0~A19	input	Address inputs
A0~A3	input	Page Address input
/CE1	input	Chip enables input 1. Low: enable
CE2	input	Chip enable input 2. High: enable, Low: enter power down mode
/WE	input	Write enable input
/OE	input	Output enable input
/LB	input	Lower byte data input/output control pin
/UB	input	Upper byte data input/output control pin
I/O0~I/O15	I/O	Data input/output pins
V_{CC}	Power	Power Supply
V_{SS}	Power	Ground
NC		No connection

Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V_{DD} Current
Deep power down	X	L	X	X	X	X	High Z	High Z	
Standby	H	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}
Upper Byte Read					L	H	D_{OUT}	High Z	I_{CC}
Lower Byte Read					H	L	High Z	D_{OUT}	I_{CC}
Write	L	H	X	L	L	L	D_{IN}	D_{IN}	I_{CC}
Upper Byte Write					L	H	D_{IN}	Invalid	I_{CC}
Lower Byte Write					H	L	Invalid	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	Voltage of V_{CC} supply relative to V_{SS}	-0.2 to Vcc+0.3	V
V_{IN} , V_{OUT}	Voltage at any pin relative to V_{SS}	-0.2 to Vcc+0.3	V
T_{STG}	Storage Temperature	-65 to +150	^{O}C
P_T	Power Dissipation	1.0	W

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (TA = -40 to + 85°C , V_{CC} = 2.6~3.6V)

Parameter Name	Parameter	Test Conduction	MIN	TYP	MAX	Unit
V_{IL}	Input Low Voltage (1)		-0.2		0.2*Vcc	V
V_{IH}	Input High Voltage (1)		0.8*Vcc		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE1=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA			0.2*Vcc	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	0.8*Vcc			V
I_{CC1}	Operating Power Supply Current	Cycle time=1us, I_{IO}=0mA, 100% duty, /CE1≦0.2V, CE2≧ Vcc-0.2V, V_{IN}≦0.2V or V_{IN}≧VCC-0.2V			5	mA
I_{CC2}		Cycle time=Min, I_{IO}=0mA, 100% duty, /CE1=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IL} or V_{IH}			25	mA
I_{CCSB1}	Standby Current -CMOS	/CE1 & CE2≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦ 0.2V			120	uA
I_{CCSB2}	Deep Power-down Standby Current	CE2 < 0.2V, Other inputs = 0 ~ VDDQ (Max. condition : VDD=3.6V @ 85oC)			20	uA

1. V_{IH}(Max) V_{CC}+1.0V with 10ns pulse width, V_{IL}(Min)-1.0V with 10ns pulse width

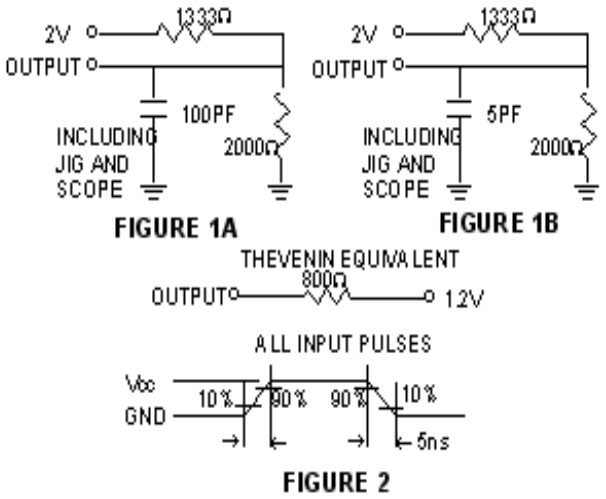
Capacitance (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{DQ}	Input /Output Capacitance	$V_{I/O}$=0V	10	pF

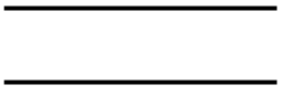
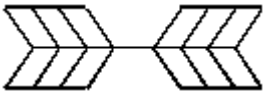
This parameter is guaranteed and not tested.

AC Test Conditions

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output	
Timing Reference Level	0.5Vcc



Key to Switching Waveforms

Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don’t care any change permitted	Change state unknown
	Does not apply	Center line is high impedance “OFF” state

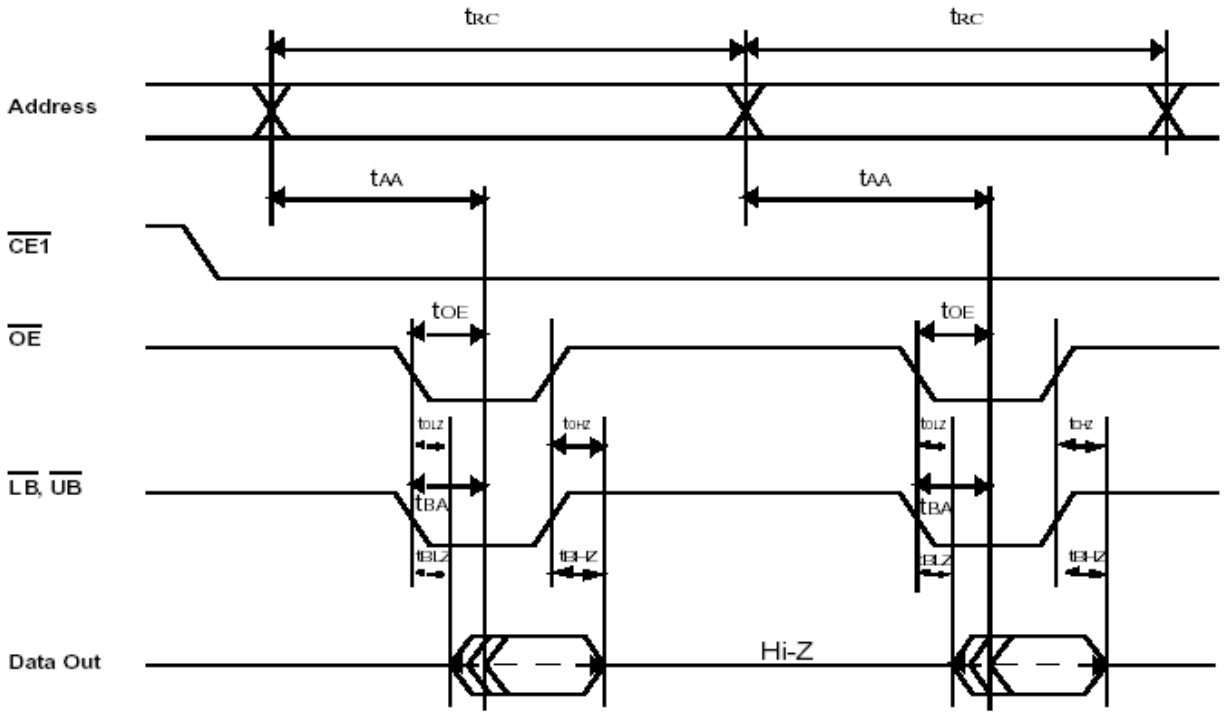
AC Characteristics (T_A = -40 to + 85°C, V_{CC}= 2.6V~3.6V)

Read cycle

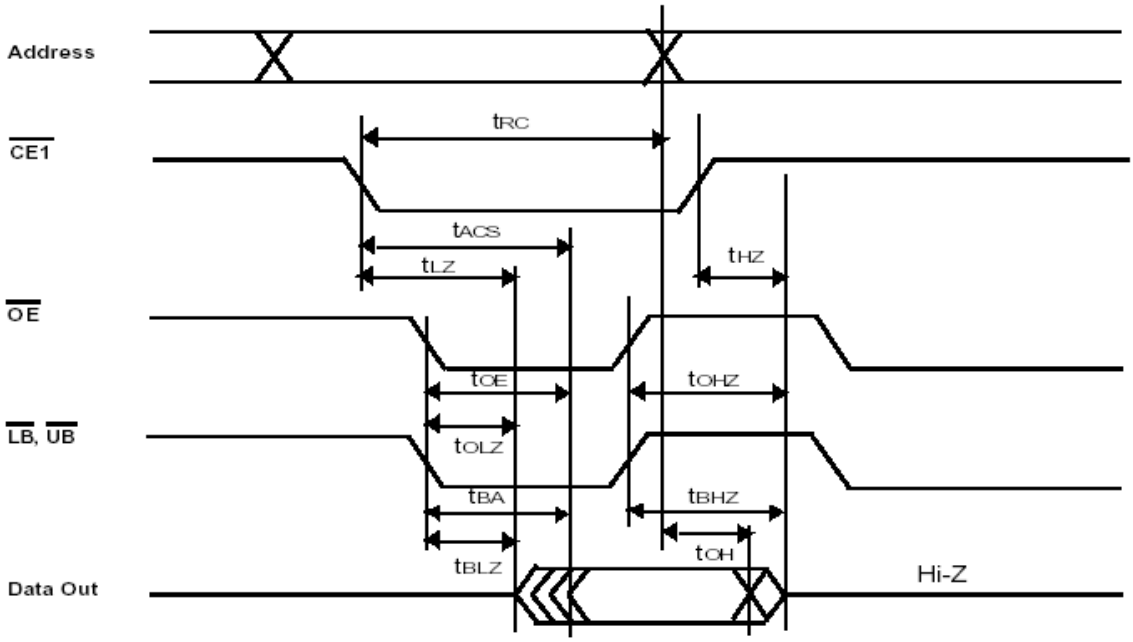
Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t_{RC}	70	10k	ns
Address access time	t_{AA}	-	70	ns
Chip enable access time (/CE1)	t_{ACS}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	25	ns
Output hold from address change	t_{OH}	5	-	ns
Chip enable to output in low Z (/CE1)	t_{LZ}*	10	-	ns
Output enable to output in low Z (/OE)	t_{OLZ}*	0	-	ns
Byte enable to output in low Z	t_{BLZ}*	0	-	ns
Chip disable to output in High Z (/CE1)	t_{HZ}*	0	20	ns
Output disable to output in High Z (OE)	t_{OHZ}*	0	20	ns
Byte disable to output in High Z	t_{BHZ}*	0	20	ns

These parameters are sampled and are not 100% tested

Read Cycle 1: /CE1 =VIL, /WE =VIH



Read Cycle 2: /WE = VIH

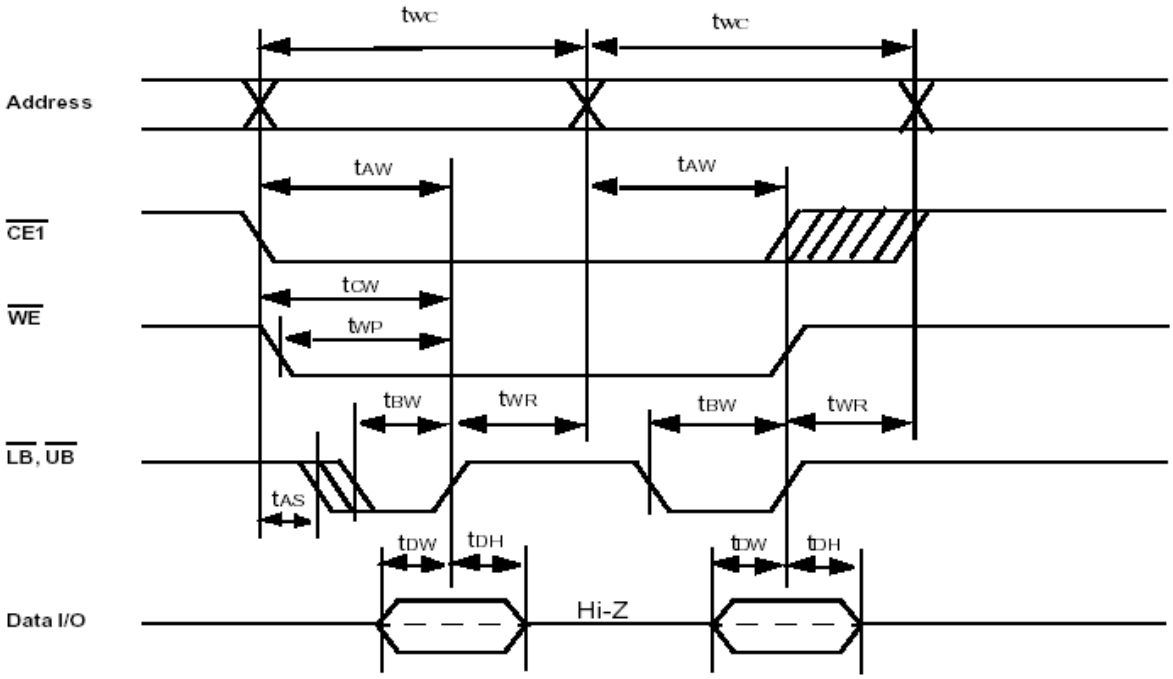


Write Cycle

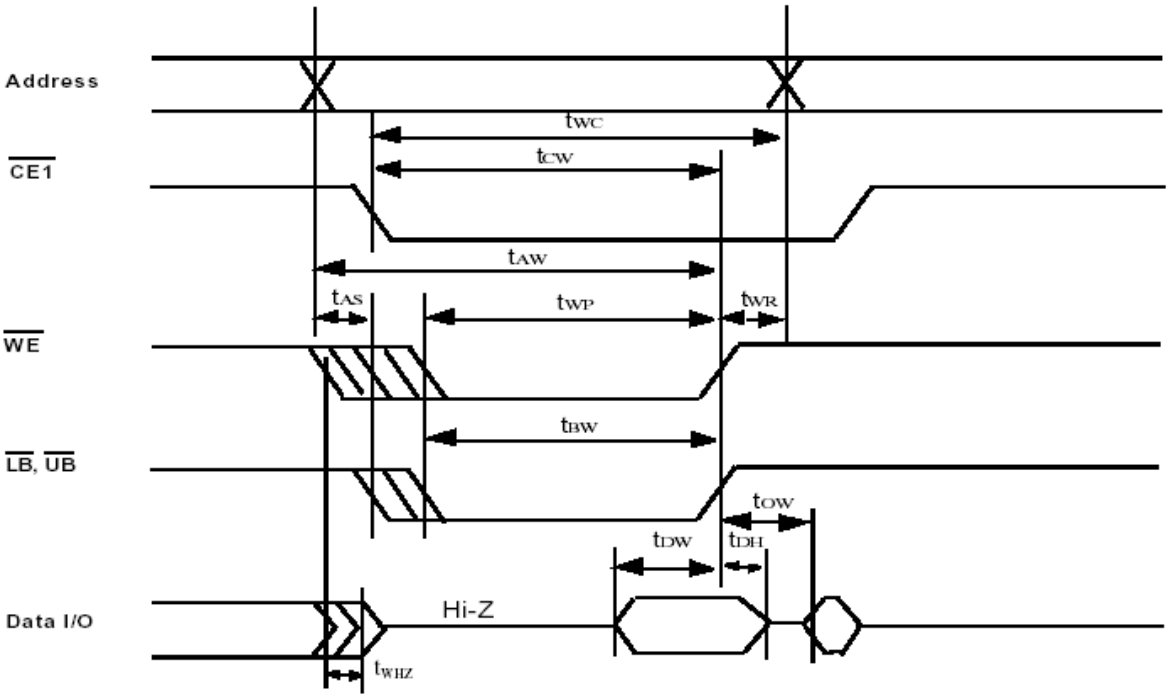
Parameter Name	Name	70		Unit
		Min	Max	
Write cycle time	t_{WC}	70	10k	ns
Byte enable to end of write	t_{BW}	60	-	ns
Address valid to end of write	t_{AW}	60	-	ns
Chip select to end of write	t_{CW}	60	-	ns
Data set up time	t_{DW}	20	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OW*}	5	-	ns
/CE1 low to output low Z	t_{Lz*}	-5	-	ns
/OE high to output high Z	t_{OHZ*}	-	15	ns
Write to output high Z	t_{WHZ*}	-	20	ns

**These parameters are sampled and are not 100% tested*

Write Cycle 1: /LB & /UB control



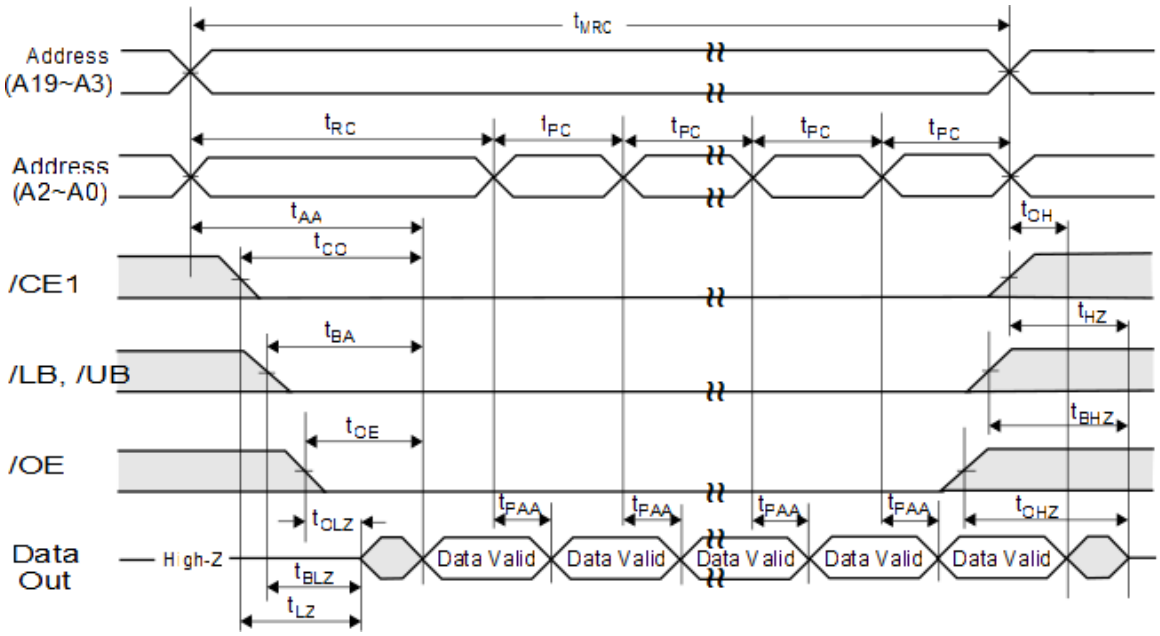
Write Cycle 2: /WE control



Page Cycle

Parameter Name	Name	Min.	Max.	Unit
Max. cycle time	t_{MRC}	-	10k	ns
Page mode cycle time	t_{PC}	25	-	ns
Page mode address access time	t_{PAA}		25	ns

Page read cycle (1) (CE2=/we=V_{IH}, 8 Words access)

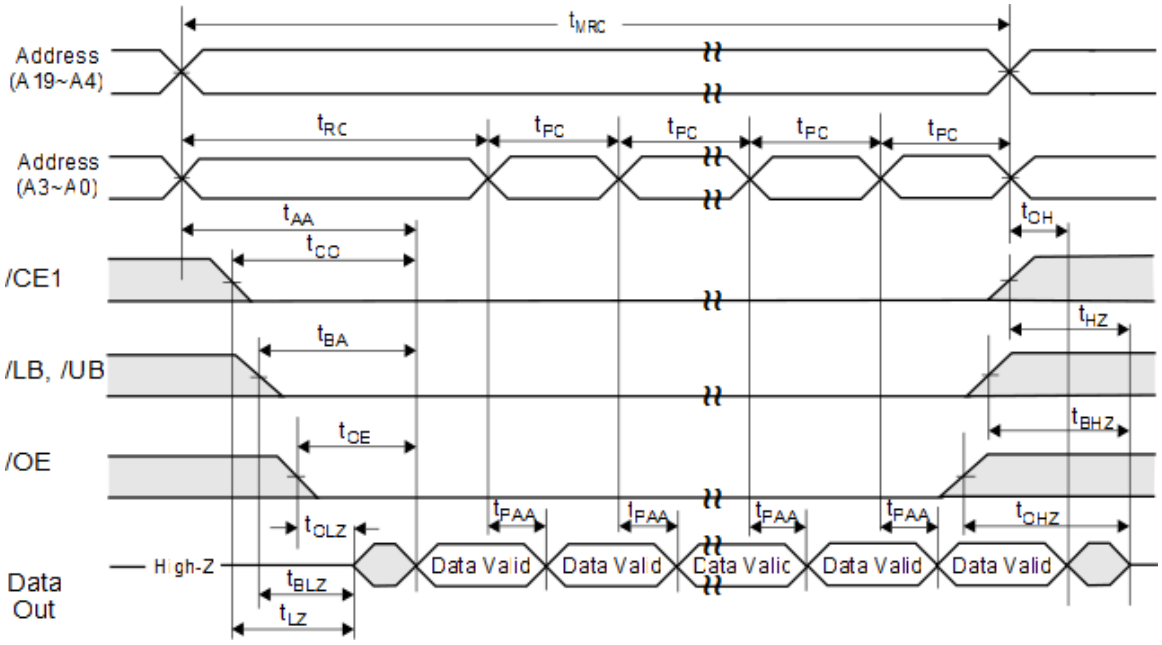


(read cycle)

1. t_{HZ}, t_{BHZ}, t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not access device with cycle timing shorter than t_{RC} for continuous periods >10us.

Page read cycle (2) (CE2=/we=V_{IH}, 16 Words access)



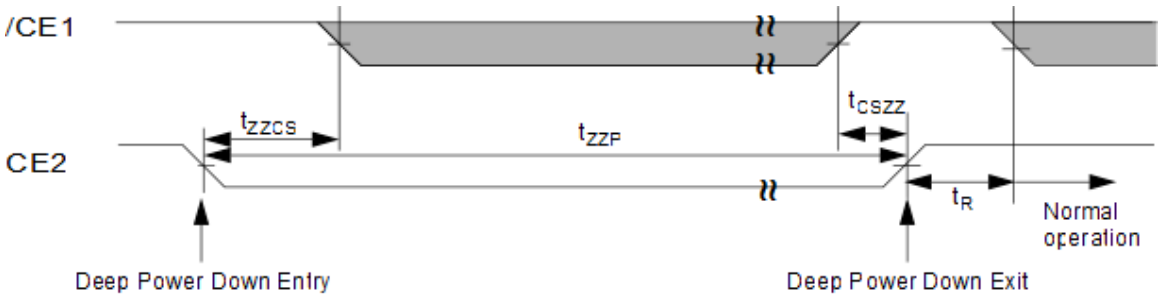
(read cycle)

1. t_{HZ}, t_{BHZ}, t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not access device with cycle timing shorter than t_{RC} for continuous periods >10us.

Low Power Modes

Deep power down mode entry/exit

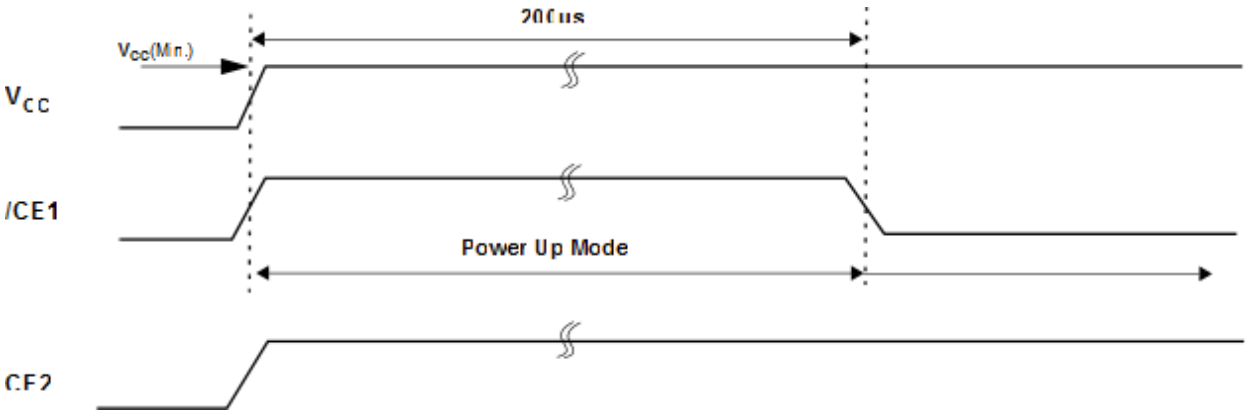


(Deep power down)

During deep power down mode, all refresh related activity is disabling.

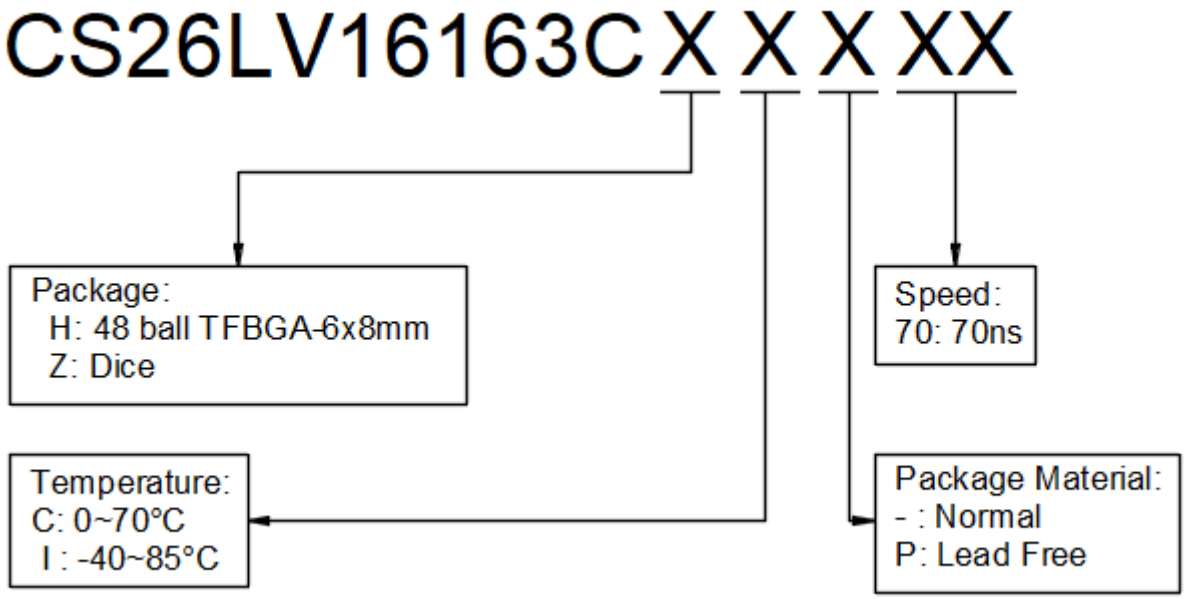
Parameter Name	Name	Min.	Max.	Unit
t_{ZZCS}	CE2 low to /CE1 low	0	-	ns
t_{CSZZ}	/CE1 high to CE2 high	0	-	ns
t_R	Operation recovery time	200	-	ns
t_{ZZP}	CE2 pulse width	20	-	ns

Timing waveform power up



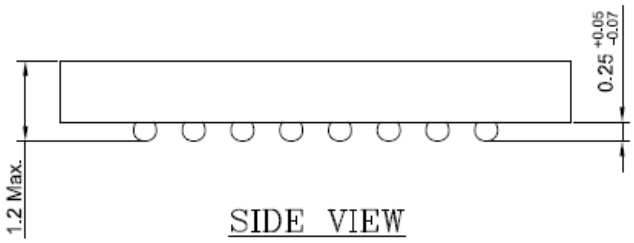
** After VCC reaches VCC (Min.), wait 200us with /CE1 high, then you get into the normal operation.*

Order Information

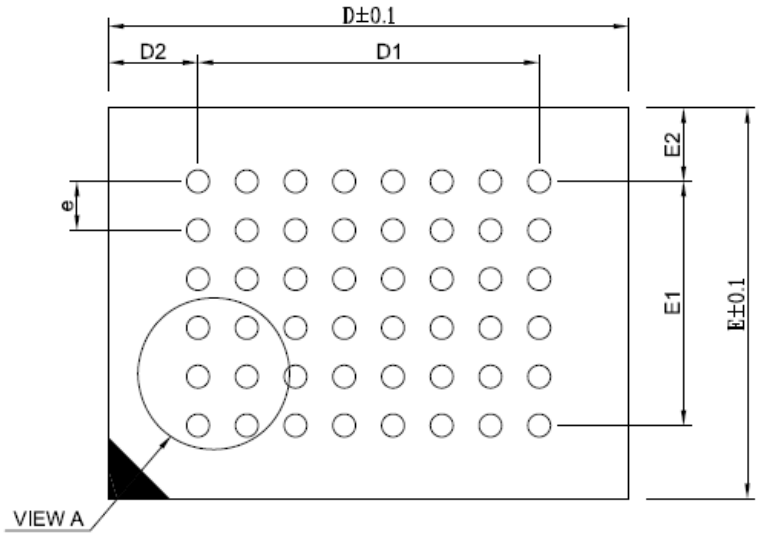


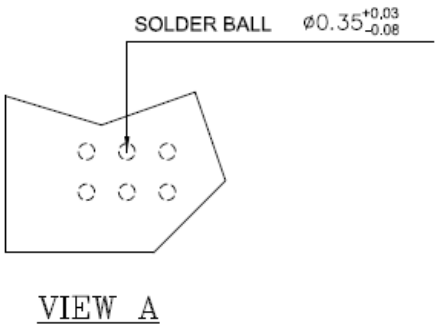
Package Outline

48 ball TFBGA-6x8mm



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125





NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:

   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025