Key Features

- VDD=VDDQ=1.2V +/- 0.06V (1.14V~1.26V)
- VPP = 2.5V, -0.125V/+0.25V
- On-die, internal, adjustable VREFDQ generation
- 1.2V pseudo open-drain I/O
- 8 internal banks (x16): 2 groups of 4 banks each
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 and 20 supported
- Programmable additive latency 0, CL-1, and CL-2 supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12, 14, 16, 18
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- Average Refresh Cycle (Tcase of 0 °C~ 95°C)
  - 7.8 µs at 0°C ~ 85°C
  - 3.9 µs at 85°C ~ 95°C
- Data strobe preamble training
- Driver strength selected by MRS
- Programmable data strobe preambles
- Dynamic On Die Termination
- Two Termination States such as RTT_PARK and RTT_NOM switchable by ODT pin
- Asynchronous RESET pin
- Internal (self) calibration: Internal self calibration through ZQ pin (RZQ: 240 ohm ± 1%)
- TDQS (Termination Data Strobe) supported (x8 only)
- Write and read leveling
- Databus write cyclic redundancy check (CRC)
- Maximum power saving mode
- Temperature controlled refresh (TCR)
- Low-power auto self refresh (LPASR)
- Fine granularity refresh
- Per-DRAM addressability
- Geardown mode
- Self refresh abort
- Command/Address (CA) parity
- Data bus inversion (DBI) for data bus
- Connectivity Test Mode (x16)
- PPR is supported
- JEDEC standard package
  - 96ball FBGA(x16)
- Lead free & RoHS compliant
- JEDEC JESD-79-4 compliant
- **Operating Temperature (Tcase)**
  - Commercial (-C) : 0°C ≤ TC ≤ 95°C
  - Industrial (-I): -40°C ≤ TC ≤ 95°C

Speed	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
	11-11-11	13-13-13	15-15-15	17-17-17	19-19-19	20-20-20	22-22-22	
tCK(min)	1.25	1.071	0.937	0.833	0.75	0.682	0.625	ns
CAS Latency	11	13	15	17	19	20	22	nCK
tRCD(min)	13.75	13.92	14.06	14.16	14.25	13.64	13.75	ns
tRP(min)	13.75	13.92	14.06	14.16	14.25	13.64	13.75	ns
tRAS(min)	35	34	33	32	32	32	32	ns
tRC(min)	48.75	47.92	47.06	46.16	46.25	45.64	45.75	ns

Addressing

Organization	1024Mbx4	512Mb x 8	256Mb x 16
Bank group	4	4	2
Bank group address	BG[1:0]	BG[1:0]	BG0
Bank per group	4	4	4
Bank address	BA[1:0]	BA[1:0]	BA[1:0]
Row address	64K (A[15:0])	32K (A[14:0])	32K (A[14:0])
Column address	1K (A[9:0])	1K (A[9:0])	1K (A[9:0])
Page Size	512B	1KB	2KB
tREFI	Tc≦85°C:7.8µs, Tc>85°C:3.9µs		
tRFC	260ns		

Package

4Gb (Org. / Package)		Dimension (mm)	Ball pitch (mm)
256Mbx16	96-ball FBGA	7.5 x 13	0.80

Ordering Information

Organization	Part No.	Speed			Package
		Clock (MHz)	Data Rate (Mb/s)	CL-TRCD-TRP	
Commercial Grade					
256Mx16	CS66DU4GQA-MC	1333	DDR4-2666	19-19-19	96-ball BGA
256Mx16	CS66DU4GQA-PC	1600	DDR4-3200	22-22-22	96-ball BGA
Industrial Grade					
256Mx16	CS66DU4GQA-MI	1333	DDR4-2666	19-19-19	96-ball BGA
256Mx16	CS66DU4GQA-PI	1600	DDR4-3200	22-22-22	96-ball BGA

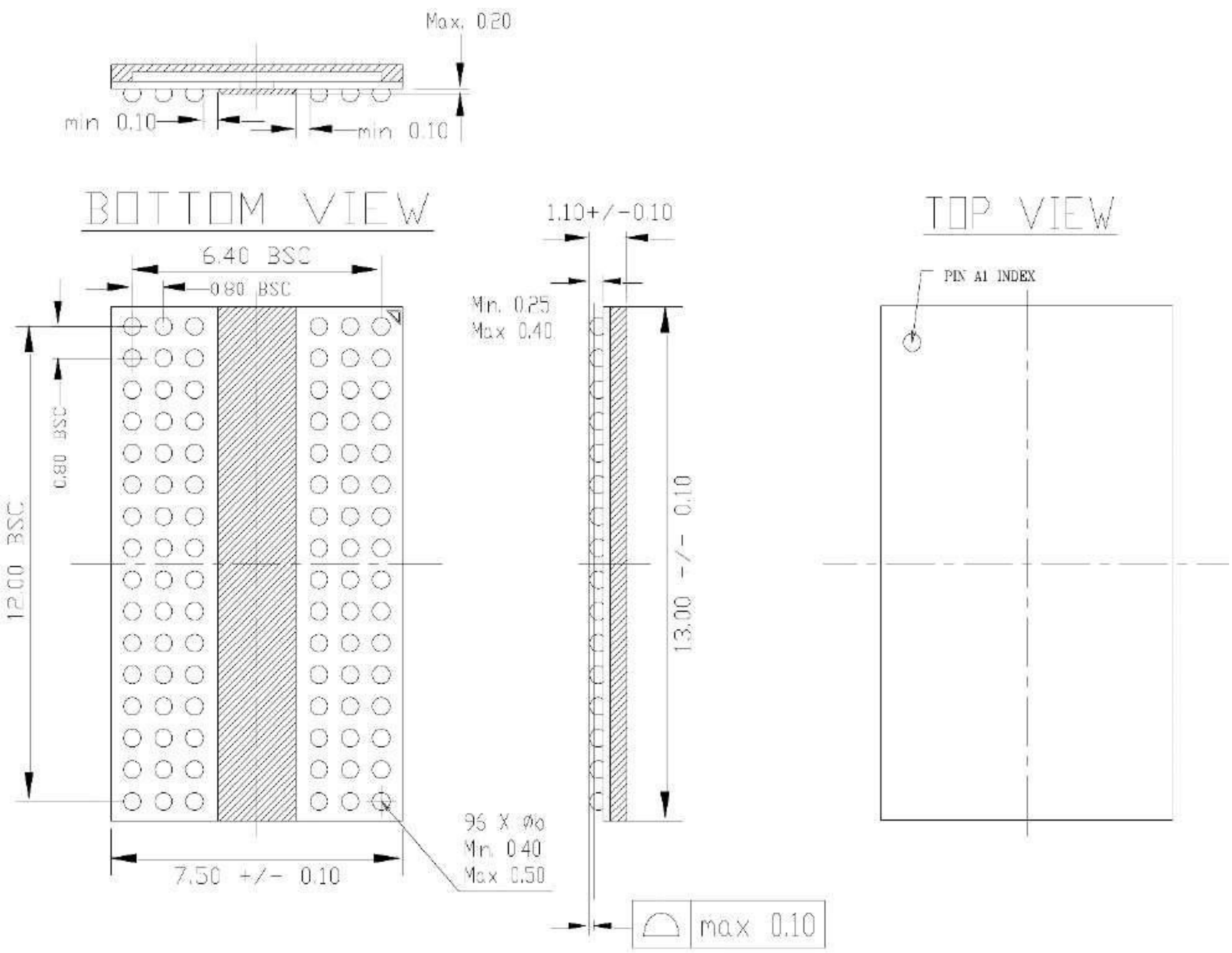
Package Ballout and Addressing

x16 Package Ballout (Top view) : 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQ9	VDD	B
C	VDDQ	DQ12	DQ10				DQ11	DQ13	VSSQ	C
D	VDD	VSSQ	DQU6				DQ15	VSSQ	VDDQ	D
E	VSS	UDM_n/ UDBI_n	VSSQ				LDM_n/ LDBI_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQ1	VDDQ	ZQ	F
G	VDDQ	DQ0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQ4	DQ2				DQ3	DQ5	VSSQ	H
J	VDD	VDDQ	DQ6				DQ7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n A14	ACT_n				CS_n	RAS_n A16	VDD	L
M	VREFCA	BG0	A10/AP				A12 BC_n	CAS_n A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

Package Dimensions

x16 96ball Package Outline Drawing



Input/Output Functional Description

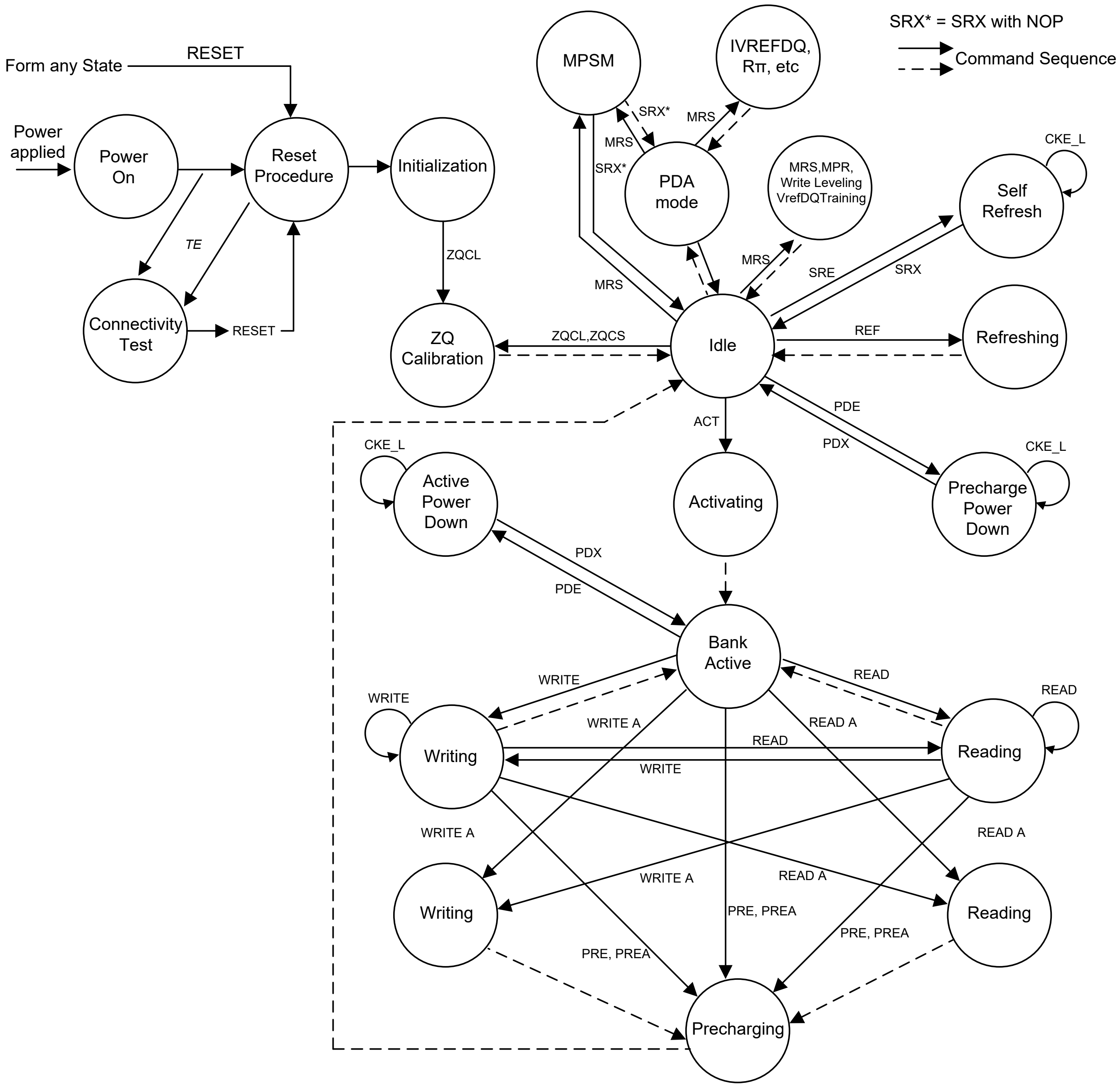
Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2 (CKE1, CS1_n, ODT1)	Input	Chip ID: These inputs are used only when devices are stacked; that is, they are used in 2H, 4H, and 8H stacks for x4 and x8 configurations (these pins are not used in the x16 configuration). DDR4 will support a traditional DDP package, which uses these three signals for control of the second die (CS1_n, CKE1, ODT1).
ODT	Input	On Die Termination: ODT (registered HIGH) enables R_{TT_NOM} termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 conurations. For x16 conuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable R_{TT_NOM}.
ACT_n	Input	Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14.
RAS_n/A16, CAS_n/A15, WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16, A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table.
DM_n/DBI_n/ TDQS_t	Input/ Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10, A11, A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifying wherther to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in x8.
BG0B- G1	Input	Bank Group Inputs: BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also detemines which mode register is to be accessed during a MRS cycle. x4/x8 have BG0 and BG1 but x16 has only BG0.
BA0B- A1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.

Symbol	Type	Function
A0-A17	Input	Address Inputs: Provied the row address for ACTIVATE Commands and the column address for Read/Write commands th select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for the x4 configration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write opera-tion. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Pre-charge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active whenRESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal VREF level during test via Mode Register Setting MR4 A4=High. During this mode, RTT value should be set to Hi-Z. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t, and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Ouput	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11, 12, 10 and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAM with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A,0 and C0- C2(3DS devices). Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW.
ALERT_n	Output	Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery trans-action to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable: Required on x16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb. HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.

Symbol	Type	Function
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activation Power Supply: 2.5V (2.375V min , 2.75 max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

NOTE : Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.

Simplified State Diagram



Abbr.	Function	Abbr.	Function	Abbr.	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bank group for x16 DRAM. The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a ‘chopped’ burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/x8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to “DDR4 SDRAM Addressing” on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode ‘on the fly’ (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

- Gear down mode (MR3 A[3]) : 0 = 1/2 Rate
- Per DRAM Addressability (MR3 A[4]) : 0 = Disable
- Max Power Saving Mode (MR4 A[1]) : 0 = Disable
- CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable
- CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable
- Hard post package repair mode (MR4 A[13]): 0 = disable
- Soft post package repair mode (MR4 A[5]): 0 = disable

Power-up Initialization Sequence

The following sequence is required for POWER UP and Initializatio.

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled “ Low” anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to VDD min must be no greater than 200ms; and during the ramp, VDD ≥ VDDQ and (VDD-VDDQ) < 0.3V. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.

   During power-up, the supply slew rate is governed by the limits stated in the table below, and either of the following conditions must be met:

Supply Power-up Slew Rate

Symbol	Min	Max	Unit	Note
VDD_SL, VDDQ_SL, VPP_SL	0.004	600	V/ms	Measured between 300mV and 80% of supply minimum
VDD_ona, VDDQ_ona	N/A	200	ms	VDD(Q) maximum ramp time from 300mV to VDD(Q) minimum

Note:20 MHz band-limited measurement

- Condition A :
  - VDD and VDDQ are driven from a single power converter output, AND
  - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.
  - VTT is limited to 0.76V max once power ramp is finished, AND
  - VREFCA tracks VDD/2.

Or

- Condition B :
  - Apply VDD without any slope reversal before or at the same time as VDDQ
  - Apply VDDQ without any slope reversal before or at the same time as VTT & VREFCA.
  - Apply VPP without any slope reversal before or at the same time as VDD.
  - The voltage levels on all pins other than VDD,VDDQ,VSS,VSSQ must be less than or equal to VDDQ and VDD on one side and must be larger than or equal to VSSQ and VSS on the other side.

2. After RESET_n is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.

3. Clocks (CK_t,CK_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered “High” after Reset, CKE needs to be continuously registered “High” until the initialization sequence is finished, including expiration of tDLLK and tZQinit

4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5nCK)]

6. Issue MRS Command to to load MR3 with all application settings, wait tMRD.

7. Issue MRS command to load MR6 with all application settings, wait tMRD.

8. Issue MRS command to load MR5 with all application settings, wait tMRD.

9. Issue MRS command to load MR4 with all application settings, wait tMRD.

10. Issue MRS command to load MR2 with all application settings, wait tMRD.

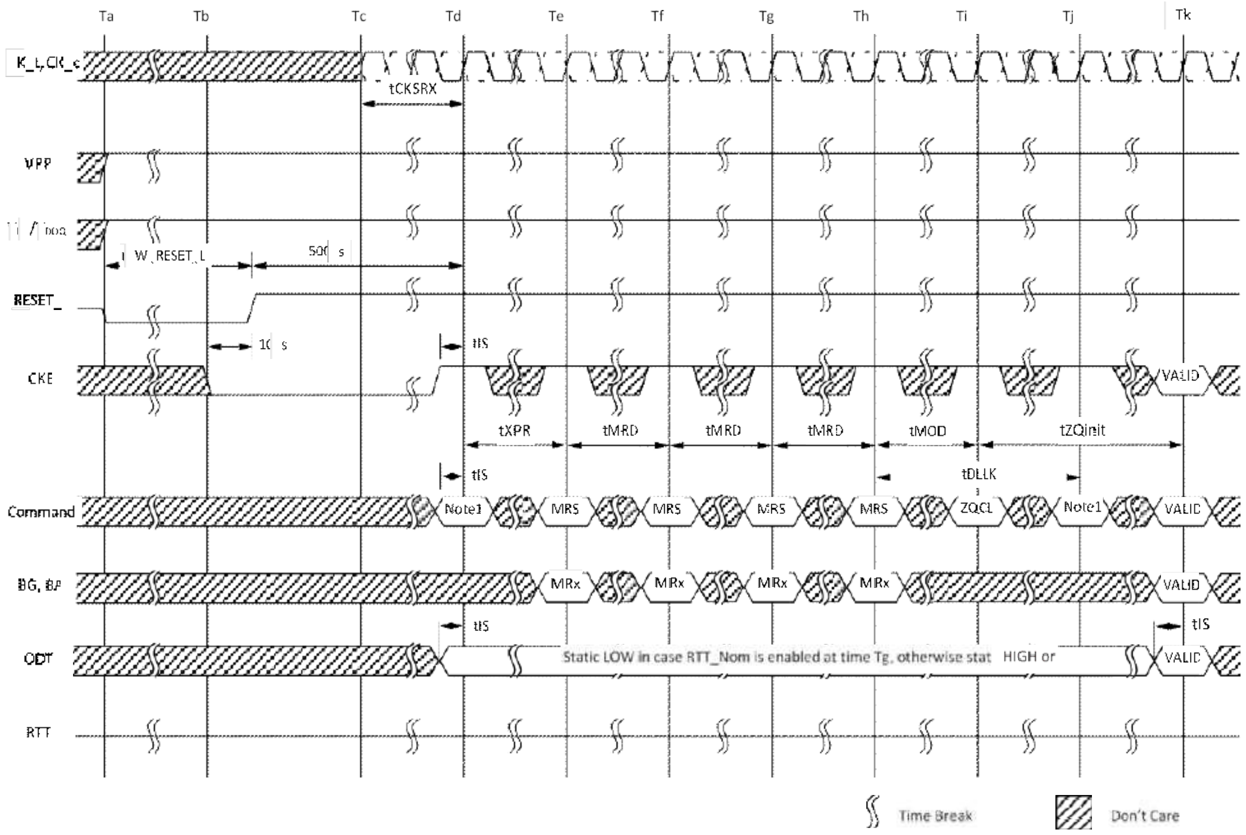
11. Issue MRS command to load MR1 with all application settings, wait tMRD.

12. Issue MRS command to load MR0 with all application settings, wait tMRD.

13. Issue ZQCL command to starting ZQ calibration

14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include VREF training and Write leveling).

RESET and Initialization Sequence at Power-On Ramping



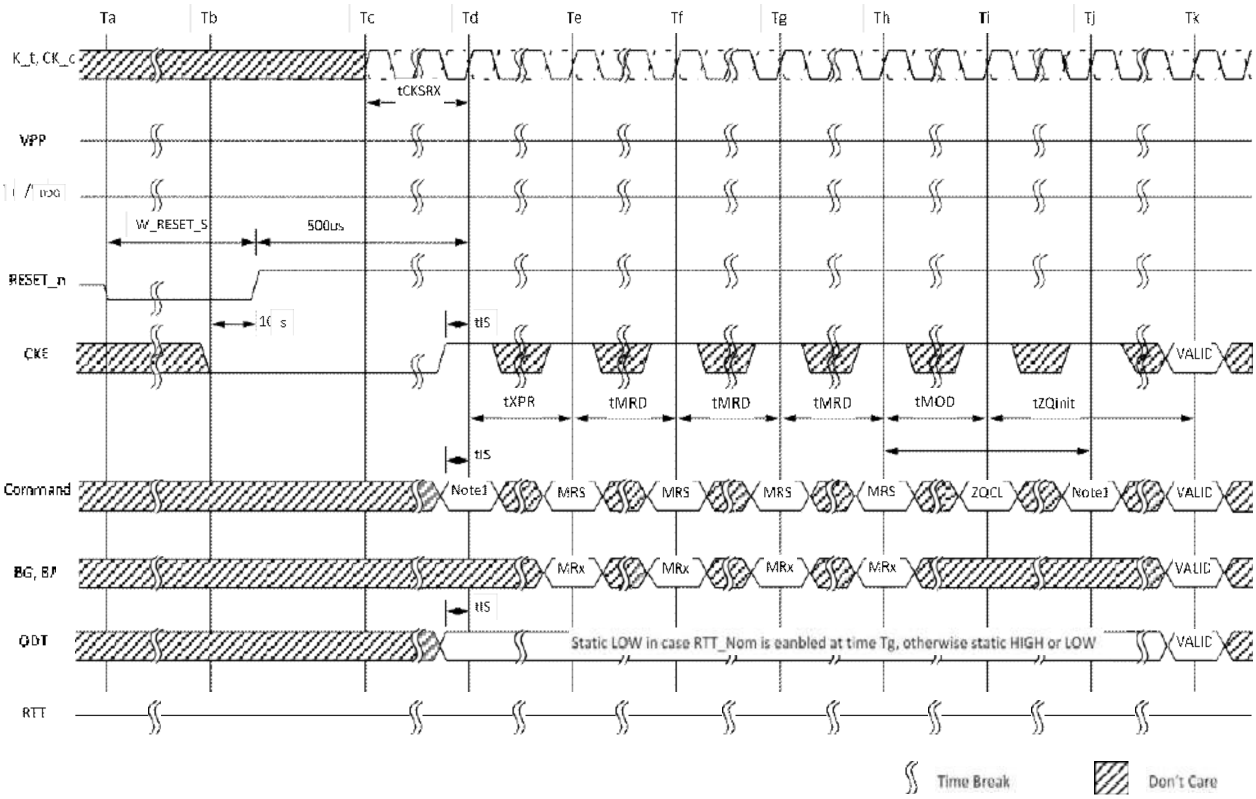
NOTE 1: From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2: MRS commands must be issued to all mode registers that have defined settings.

RESET Initialization with Stable Power Sequence

The following sequence is required for RESET at no power interruption initialization:

1. Assert RESET_n below 0.2 × VDD any time reset is needed (all other inputs may be undefined). RESET must be maintained for a minimum of 100ns. CKE is pulled LOW before RESET_n is de-asserted (minimum time 10ns).
2. Follow Steps 2 to 10 in the Reset and Initialization Sequence at Power-on Ramping procedure.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include V_{REF} training and Write leveling)

RESET Procedure at Power Stable Condition



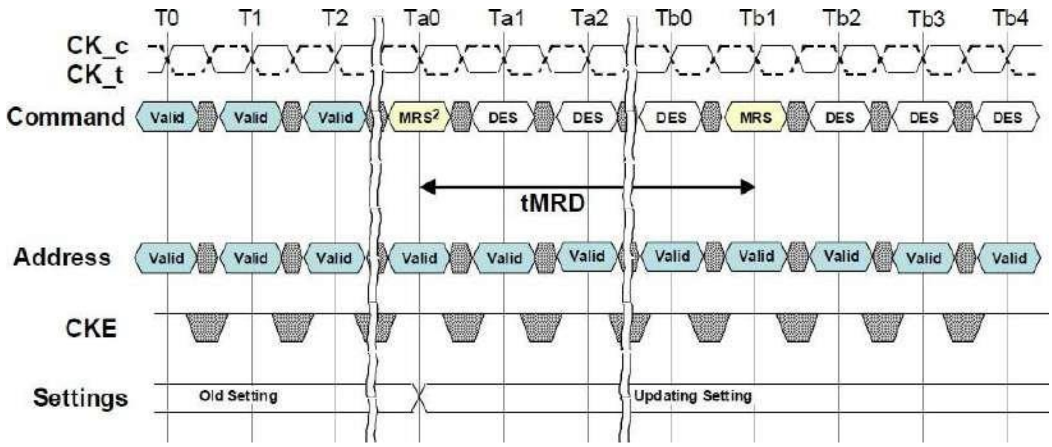
NOTE 1 From the time point Td until Tk, a DES command must be applied between MRS and ZQCL commands.
NOTE 2 MRS commands must be issued to all mode registers that have defined settings.

Programming Mode Registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers (MRn), provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS and DLL RESET commands do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. MRS Commands can be issued only when DRAM is at idle state. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in the tMRD Timing figure.

Some of the mode register settings affect address/command/control input functionality. In these cases, the next MRS command can be allowed when the function being updated by the current MRS command is completed. These MRS commands don't apply tMRD timing to the next MRS command; however, the input cases have unique MR setting procedures, so refer to individual function descriptions.

tMRD Timing



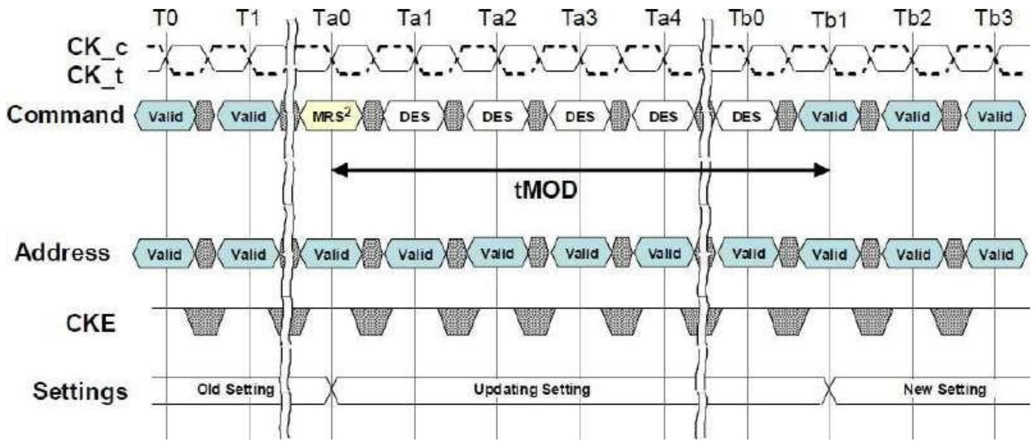
NOTE 1 This timing diagram depicts CA Parity Mode "Disabled" case.

NOTE 2 tMRD applies to all MRS commands with the following exceptions:

- Geardown Mode
- CA Parity Lantency Mode
- CS to Command/Address Lantency Mode
- Per DRAM Addressability Mode
- VREFDQ training value, VREFDQ training mode, and VREFDQ Training Range

The MRS command to non-MRS command delay, tMOD, is required for the DRAM to update features, except DLL RESET, and is the minimum time required from an MRS command to a non-MRS command, excluding DES, as shown in the tMOD Timing figure.

tMOD Timing



NOTE 1 This timing diagram depicts CA Parity Mode "Disabled" case.

NOTE 2 List of MRS commands exception that do not apply to tMOD.

- DLL Enable, DLL Reset
- VREFDQ training value, internal VREF monitor, VREFDQ training mode, and VREFDQ Training Range
- Geardown Mode
- Per DRAM Addressability Mode
- Maximum Power Saving Mode
- CA Parity Mode

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the device is in idle state; that is, all banks are in the precharged state with tRP satisfied, all data bursts are completed, and CKE is HIGH prior to writing into the mode register. If the RTT_NOM feature is enabled in the mode register prior to and/or after an MRS command, the ODT signal must continuously be registered LOW, ensuring RTT is in an off state prior to the MRS command. The ODT signal may be registered HIGH after tMOD has expired. If the RTT_NOM feature is disabled in the mode register prior to and after an MRS command, the ODT signal can be registered either LOW or HIGH before, during, and after the MRS command. The mode registers are divided into various fields depending on functionality and modes.

In some mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to the next valid command, excluding DES. These MRS command input cases have unique MR setting procedures, so refer to individual function descriptions.

Mode Register

Mode Register 0 (MR0)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A13,A11:A9	WR and RTP [2, 3]	See Table : Write Recovery and Read to Precharge
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A6:A4,A2	CAS Latency4	See Table: CAS Lantency
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE
1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge) min in clock cycles is calculated by following rounding algorithm. The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given CAS Latency. For actual supported CAS Latency, please refer to speed bin tables for each frequency. CAS Latency controlled by A12 is optional for 4Gb device.
5. A13 for WR and RTP setting is optional for 4Gb device.

Write Recovery and Read to Precharge (cycles)

A13	A11	A10	A9	WR	RTP	WR_CRC_DM
0	0	0	0	10	5	TBD
0	0	0	1	12	6	TBD
0	0	1	0	14	7	TBD
0	0	1	1	16	8	TBD
0	1	0	0	18	9	TBD
0	1	0	1	20	10	TBD
0	1	1	0	24	12	TBD
0	1	1	1	22	11	Reserved
1	0	0	0	26	13	

CAS Latency

A12	A6	A5	A4	A2	CAS Latency	Note
0	0	0	0	0	Reserved	1
0	0	0	0	1	Reserved	
0	0	0	1	0	11	1
0	0	0	1	1	12	
0	0	1	0	0	13	1
0	0	1	0	1	14	
0	0	1	1	0	15	1
0	0	1	1	1	Reserved	
0	1	0	0	0	18	
0	1	0	0	1	20	
0	1	0	1	0	22	
0	1	0	1	1	24	
0	1	1	0	0	Reserved	1
0	1	1	0	1	17	1
0	1	1	1	0	19	1
0	1	1	1	1	Reserved	1
1	0	0	0	0	Reserved	
1	0	0	0	1	Reserved	
1	0	0	1	0	Reserved	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	0	1	0	1	Reserved	
1	0	1	1	0	Reserved	
1	0	1	1	1	Reserved	
1	1	0	0	0	Reserved	

Note 1: This CL setting is related to read DBI usage only and please check “Speed bin” section and have a proper corresponding option to use.

Mode Register 1 (MR1)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW [3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff [1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	See Table: RTT_NOM
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency	00 = 0 (AL disabled) 01 = CL-1 10 = CL-2 11 = Resrved
A2, A1	Output Driver Impedance Control	See Table: Output Driver Impedance Control
A0	DLL Enable	0 = Disable [2] 1 = Enable

NOTE

1. Outputs disabled -DQs, DQS_ts, DQS_cs.
2. States reversed to “0 as Disable” with respect to DDR4.
3. Reserved for Register control word setting.DRAM ignores MR command with BG0,BA[1:0]=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	Disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7 (34 ohm)
0	1	RZQ/5 (48 ohm)
1	0	Reserved
1	1	Reserved

Mode Register 2 (MR2)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11:A9	R_{TT_WR}	See Table: R_{TT_WR}
A8	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	See Table: CWL (CAS Write Latency)
A2:A0	RFU	0 = must be programmed to 0 during MRS

NOTE 1. Reserved for Register control word setting. DRAM ignores MR command with BG0, BA[1:0]=111 and doesn't respond.
When RFU MR code setting is inputted, DRAM operation is not defined.

RTT_WR

A11	A10	A9	RTT_WR
0	0	0	Dynamic ODT Off
0	0	1	RZQ/2 (120 ohm)
0	1	0	RZQ/1 (240 ohm)
0	1	1	Hi-Z
1	0	0	RZQ/3 (80 ohm)
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

CAS Write Latency (CWL)

A5	A4	A3	CWL	Speed bin in MT/s	
				1tCK WRITE preamble	2tCK WRITE preamble[1]
0	0	0	9	1600	
0	0	1	10	1866	
0	1	0	11	2133/1600	
0	1	1	12	2400/1866	
1	0	0	14	2666/2133	2400
1	0	1	16	2933, 3200/2400	2666/2400
1	1	0	18	2666	2933, 3200/2666
1	1	1	20	2933, 3200	2933, 3200

NOTE 1: The 2Tck WRITE preamble is valid for DDR4-2400/2666/2933 Speed Grade. For the 2nd Set of 2Tck WRITE preamble, no additional CWL is needed.

Mode Register 3 (MR3)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A11	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved
A10:A9	Write CMD Latency when CRC and DM are enabled	See Table: Write Command Latency when CRC and DM are both enabled
A8:A6	Fine Granularity Refresh Mode	See Table: Fine Granularity Refresh Mode
A5	Temperature sensor readout	0 : Disable 1: Enable
A4	Per DRAM Addressability	0 = Disable 1 = Enable
A3	Geardown Mode	0 = 1/2 Rate 1 = 1/4 Rate
A2	MPR Operation	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 01 = Page1 10 = Page2 11 = Page3 See Table: MPR Data Format

NOTE 1: Reserved for Register control word setting.DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on-the-fly 1x/2x
1	1	0	Enable on-the-fly 1x/4x
1	1	1	Reserved

Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866, 2133, 2400, 2666
1	0	6nCK	2933, 3200
1	1	Reserved	Reserved

NOTE

1. The WRITE command latency (WCL) must be set when both write CRC and DM are enabled for write CRC persistent mode
2. At less than or equal to 1600 then 4nCK; neither 5nCK nor 6nCK
3. At greater than 1600 and lessthan or equal to 2666 then 5nCK; neither 4nCK nor 6nCK
4. At greater than 2666 and less than or equal to 3200 then 6nCK; neither 4nCK nor 5nCK

MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>Note</th></tr>
<tr><td rowspan="5">BA1:BA0</td><td>00 = MPR0</td><td>A[7]</td><td>A[6]</td><td>A[5]</td><td>A[4]</td><td>A[3]</td><td>A[2]</td><td>A[1]</td><td>A[0]</td><td rowspan="5">Read only</td></tr>
<tr><td>01 = MPR1</td><td>CAS_n/ A15</td><td>WE_n/ A14</td><td>A[13]</td><td>A[12]</td><td>A[11]</td><td>A[10]</td><td>A[9]</td><td>A[8]</td></tr>
<tr><td>10 = MPR2</td><td>PAR</td><td>ACT_n</td><td>BG[1]</td><td>BG[0]</td><td>BA[1]</td><td>BA[0]</td><td>A[17] [3]</td><td>RAS_n/ A16</td></tr>
<tr><td rowspan="2">11 = MPR3</td><td rowspan="2">CRC Error Status</td><td rowspan="2">CA Parity Error Status</td><td colspan="3">CA Parity Latency [4]</td><td rowspan="2"></td><td rowspan="2"></td><td rowspan="2"></td></tr>
<tr><td>MR5.A[2]</td><td>MR5.A[1]</td><td>MR5.A[0]</td></tr>
</table>

NOTE

1. MPR used for C/A parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. MPR page 1 used for CA parity error log readout is enabled by setting A[2] in MR3.
4. MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	hPPR	sPPR	RTT_WR	Temperature Sensor Status		CRC Write Enable	RTT_WR		Read only
		-	-	MR2	-	-	MR2	MR2		
		-	-	A11	-	-	A12	A10	A9	
	01= MPR1	VREF DQ Traing range	VREF DQ training Value						Gear down Enable	
		MR6	MR6							
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency					CAS Write Latency			
		MR0					MR2			
		A6	A5	A4	A2	A12	A5	A4	A3	
	11 = MPR3	RTT_NOM			RTT_PARK			Driver Impedance		
		MR1			MR5			MR1		
		A10	A9	A6	A8	A7	A6	A2	A1	

MR bit for Temperature

MR3 bit A5=1: DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.

MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2 x tREFI)
1	1	Reserved

MPR page3 (Vendor use only)[1]

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Note
BA1:BA0	00 = MPR0	don't care								Read only
	01 = MPR1	don't care								
	10 = MPR2	don't care								
	11 = MPR3	don't care								

NOTE 1 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

Mode Register 4 (MR4)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	hPPR	0 = Disable 1 = Enable
A12	Write Preamble	0 = 1 nCK 1 = 2 nCK
A11	Read Preamble	0 = 1 nCK 1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable 1 = Enable
A9	Self Refresh Abort	0 = Disable 1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 100 = 6 101 = 8 110 = Reserved 111 = Reserved (See Table: CS to CMD/ADDR Latency Mode Setting)
A5	sPPR	0 = Disable 1 = Enable
A4	Internal VREF Monitor	0 = Disable 1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable 1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal 1 = Extended
A1	Maximum Power Down Mode	0 = Disable 1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.
When RFU MR code setting is inputted, DRAM operation is not defined.

CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

Mode Register 5 (MR5)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable 1 = Enable
A8:A6	RTT_PARK	See Table: RTT_PARK
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	CA Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	CA Parity Latency Mode	See Table: CA Parity Latency Mode

NOTE

1. Reserved for Register control word setting.DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

CA Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600/1866/2133
0	1	0	5	2400/2666
0	1	1	6	2933/3200
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmeaccording to timing parameters by speed grade table.

Mode Register 6 (MR6)

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3 100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	See Table: tCCD_L & tDLLK
A9, A8	RFU	0 = must be programmed to 0 during MRS
A7	VREFDQ Training Enable	0 = Disable(Normal operation Mode) 1 = Enable(Training Mode)
A6	VREFDQ Training Range	0 = Range 1 1 = Range 2
A5:A0	VREFDQ Training Value	See Table: VREFDQ Training Values

NOTE 1 Reserved for Register control word setting.DRAM ignores MR command with BG0,BA[1:0]=111 and doesn't respond.

tCCD_L & tDLLK

A12	A11	A10	tCCD_L.min (nCK)[1]	tDLLKmin (nCK)[1]	Note
0	0	0	Reserved	597	≤ 1333Mbps
0	0	1	5		>1333Mbps and ≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	>1866Mbps and ≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	>2400Mbps and ≤ 2666Mbps (2666Mbps)
1	0	0	8		>2666Mbps and ≤ 3200Mbps (2933/3200Mbps)
1	0	1	Reserved		
1	1	0			
1	1	1			

NOTE 1 tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency.

VREFDQ Training Values

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	-75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 111111	Reserved	Reserved

Mode Register 7 (MR7)

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

Command Description and Operation

Command Truth Table

Note 1,2,3 and 4 apply to the entire Command truth table

Note 5 applies to all Read/Write commands.

[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don’t Care, V=Valid H or L].

Function	Symbol	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Prev.	Pres.													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE

1. All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When ACT_n = H; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14 respectively.
2. RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.

6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Controller guarantees self refresh exit to be synchronous.
9. VPP and VREF(VREFCA) must be maintained during Self Refresh operation.
10. Mode Exit
11. Refer to the CKE Truth Table for more detail with CKE transition.
12. During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

CKE Truth Table

Current State[2]	CKE		Command (N)[3] RAS_n, CAS_n, WE_n, CS_n	Action (N)[3]	NOTE
	Previous Cycle[1] (N-1)	Present Cycle[1] (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE
1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are DESELECT only.
12. Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See “Self-Refresh Operation” and See “Power-Down Modes”.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VPP and VREF(VREFCA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc).

Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table below. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on-the-fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC_n.

Burst Length	Read/ Write	Starting Column Address (A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0, V, V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1, V, V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V, V, V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC_n, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. Output driver for data and strobes are in high impedance.
4. V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X : Don't Care.

BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1:A0=0:0:0] when write CRC is enabled in BL8 (fixed).

DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”. The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to “Input clock frequency change”.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

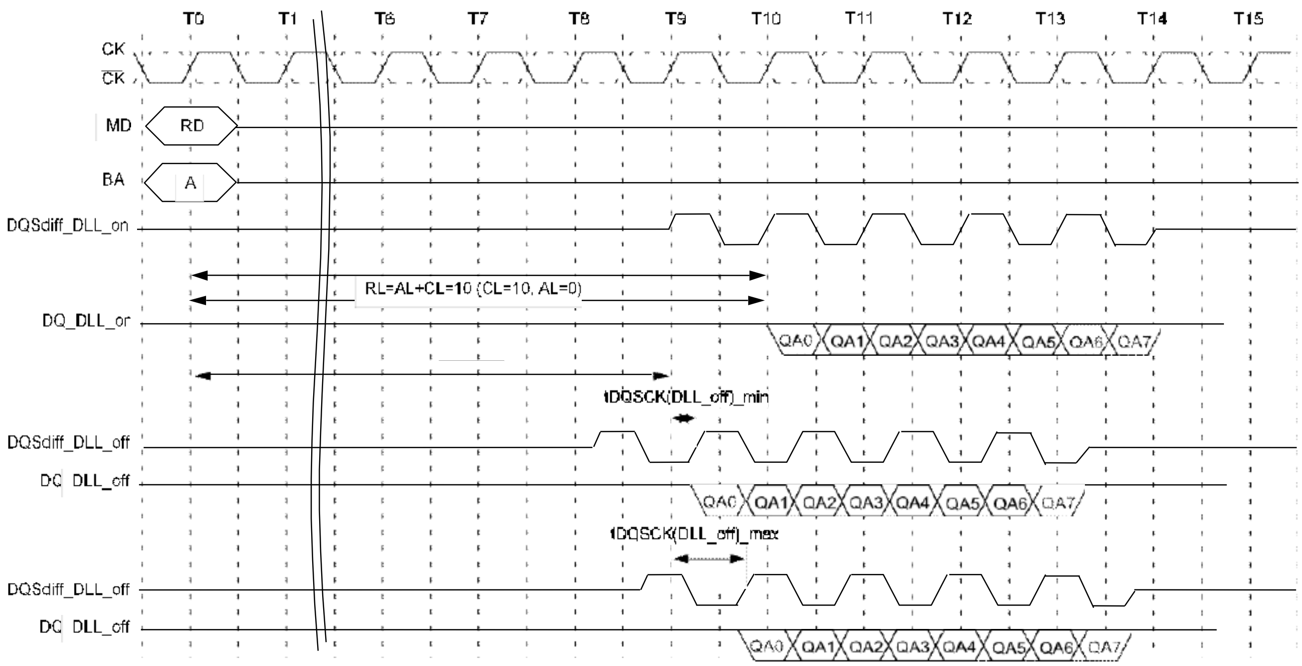
DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Compared with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.

Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode. The tDQSCK(DLL_off) values are vendor specific.

The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram (CL=10, BL=8, PL=0):

DLL-Off Mode Read Timing Operation



DLL On/Off Switching Procedure

DDR4 DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until the A0 bit is set back to “1”.

DLL On to DLL Off Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during self refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, R_{TT_NOM}, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to “0” to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with “Input clock frequency change” on Section 4.6.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t Care.
8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).

   - tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8

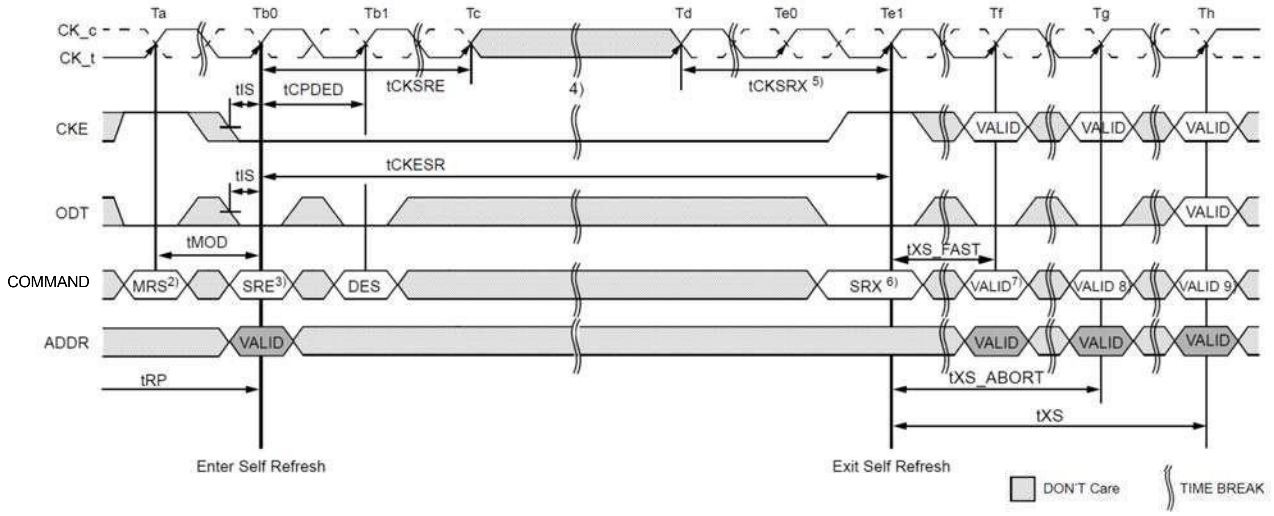
   - tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in

   MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressibility mode. Access to other DRAM mode registers must satisfy tXS timing.

   - tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter.

   The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
9. Wait for tMOD, and then the DRAM is ready for the next command.

DLL Switch Sequence from DLL On to DLL Off



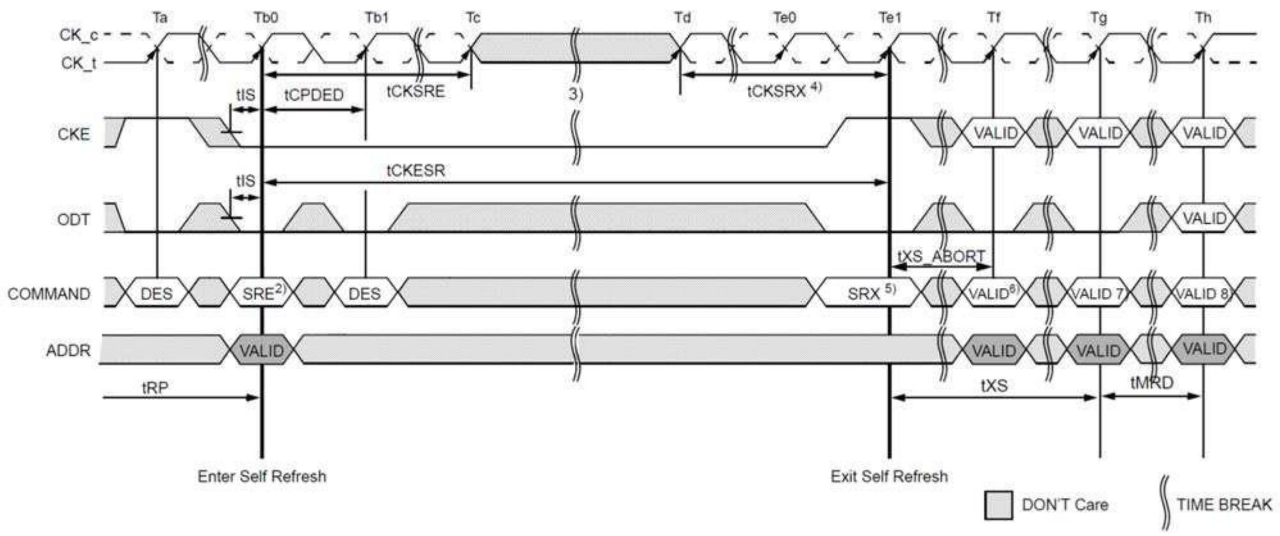
NOTE
1. Starting with idle state. RTT in stable.
2. Disable DLL by setting MR1 bit A0 to “0”.
3. Enter SR.
4. Change frequency.
5. Clock must be stable in tCKSRX.
6. Exit SR.
7. Update mode registers allowed with DLL_off parameters setting.

DLL Off to DLL On Procedure

To switch from DLL off to DLL on (with required frequency change) during self refresh:

1. Starting from the idle state (all banks pre-charged, all timings fulfilled, and DRAM on-die termination resistors (RTT_NOM) must be in the high impedance state before self refresh mode is entered.)
2. Enter Self Refresh mode; wait until tCKSRE satisfied.
3. Change frequency, following the guidelines in the “Input Clock Frequency Change” section.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from the subsequent DLL RESET command is satisfied. In addition, if any ODT features were enabled in the mode registers when self refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from the subsequent DLL RESET command is satisfied. If RTT_NOM was disabled in the mode registers when self refresh mode was entered, the ODT signal is "Don't Care."
6. Wait tXS or tXS_ABORT, depending on bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.
8. Wait tMRD, then set mode registers with appropriate values (especially an update of CL, CWL, and WR may be necessary. After tMOD is satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for the next command. (Remember to wait tDLLK after DLL RESET before applying any command requiring a locked DLL.) In addition, wait for tZQoper in case a ZQCL command was issued.

DLL Switch Sequence from DLL Off to DLL On



NOTE
1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6. Set DLL-on by MR1 A0=’1’
7. Start DLLReset
8. Update rest MR register values after tDLLK (not shown in the diagram)
9. Ready for valid command after tDLLK (not shown in the diagram)

Input Clock Frequency Change

After the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications. The input clock frequency can be changed from one stable clock rate to another stable clock rate only when in self refresh mode. Outside of self refresh mode, it is illegal to change the clock frequency.

After the DDR4 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in “Self-Refresh Operation”.

For the new clock frequency, additional MRS commands to MR0, MR2, MR3, MR4, MR5, and MR6 may need to be issued to program appropriate CL, CWL, Gear-down mode, Read & Write Preamble, Command Address Latency (CAL Mode), Command Address Parity (CA Parity Mode), and tCCD_L/tDLLK value.

In particular, the Command Address Parity Latency (PL) must be disabled when the clock rate changes, ie. while in Self Refresh Mode. For example, if changing the clock rate from DDR4-2133 to DDR4-2933 with CA Parity Mode enabled, MR5[2:0] must first change from PL = 4 to PL = disable prior to PL = 6. A correct procedure would be to (1) change PL = 4 to disable via MR5 [2:0], (2) enter Self Refresh Mode, (3) change clock rate from DDR4-2133 to DDR4-2933, (4) exit Self Refresh Mode, (5) Enable CA Parity Mode setting PL = 6 via MR5 [2:0].

If the MR settings that require additional clocks are updated after the clock rate has been increased, i.e. after exiting self refresh mode, the required MR settings must be updated prior to removing the DRAM from the IDLE state, unless the DRAM is RESET. If the DRAM leaves the idle state to enter self refresh mode or ZQ Calibration, the updating of the required MR settings may be deferred to after the next time the DRAM enters the IDLE state.

If MR6 is issued prior to Self Refresh Entry for new tDLLK value, then DLL will relock automatically at Self Refresh Exit. However, if MR6 is issued after Self Refresh Entry, then MR0 must be issued to reset the DLL.

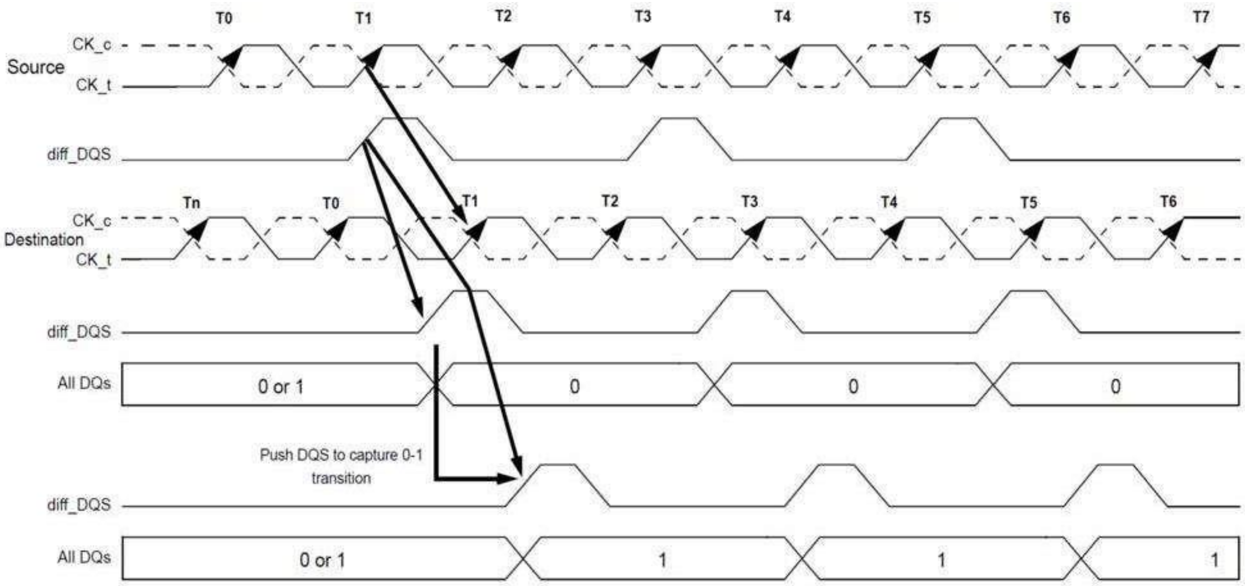
The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on mode to DLL_off mode transition sequence (see DLL On/Off Switching Procedure).

Write Leveling

For better signal integrity, DDR4 memory modules use fly-by topology for the commands, addresses, control signals, and clocks. Fly-by topology has benefits from the reduced number of stubs and their length, but it also causes flight-time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the controller to maintain tDQSS, tDSS, and tDSH specifications. Therefore, the device supports a write leveling feature to allow the controller to compensate for skew. This feature may not be required under some system conditions, provided the host can maintain the tDQSS, tDSS, and tDSH specifications.

The memory controller can use the write leveling feature and feedback from the device to adjust the DQS (DQS_t, DQS_c) to CK (CK_t, CK_c) relationship. The memory controller involved in the leveling must have an adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established though this exercise would ensure the tDQSS specification. Besides tDQSS, tDSS and tDSH specifications also need to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the AC Timing Parameters section in order to satisfy tDSS and tDSH specifications. A conceptual timing of this scheme is shown below.

Write Leveling Concept



DQS_t - DQS_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

DRAM Setting for Write Leveling and DRAM Termination Function in that Mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low'. Note that in write leveling mode, only DQS_t/DQS_c terminations are activated and deactivated via ODT pin, unlike normal operation.

MR Settings for Leveling Procedures

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

DRAM Termination Function in Leveling Mode

ODT pin at DRAM	DQS_t/DQS_c termination	DQs termination
RTT_NOM with ODT HIGH	On	Off
RTT_PARK with ODT LOW	On	Off

NOTE

1. In write-leveling mode with its output buffer disabled (MR1[bitA7] = 1 with MR1[bitA12]=1) all RTT_NOM and RTT_PARK settings are allowed; in write-leveling mode with itsoutput buffer enabled (MR1[bitA7] = 1 with MR1[bitA12] = 0) all RTT_NOM and RTT_PARK settingsare allowed.
2. Dynamic ODT function is not available in Write Leveling Mode. DRAM MR2 bits A[11:9] must be '000' prior to entering Write Leveling Mode.

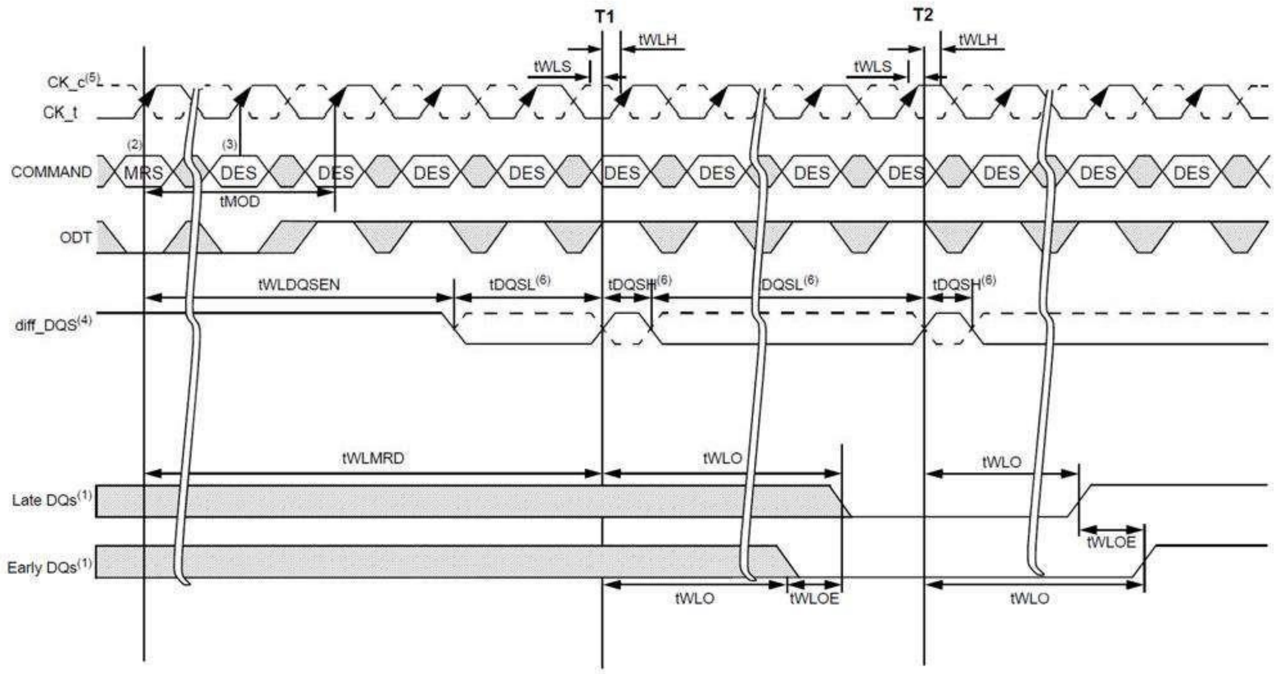
Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1 [A12]) and an MRS command to exit write leveling (MR1 [A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1 [A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS_t low and DQS_c high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge which is used by the DRAM to sample CK_t - CK_c driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK_t - CK_c status with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/DQS_c) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next DQS_t/DQS_c pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS_t - DQS_c delay setting and write leveling is achieved for the device.

Write Leveling Sequence (DQS Capturing CK LOW at T1 and CK HIGH at T2)



NOTE

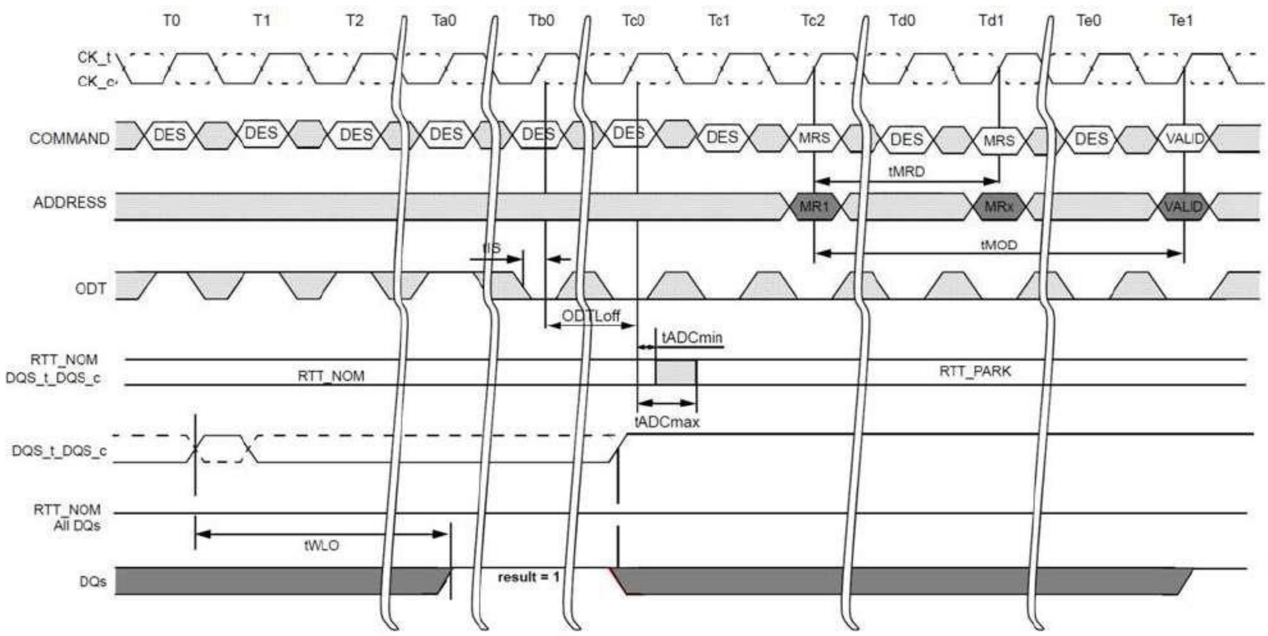
1. The device drives leveling feedback on all DQs.
2. MRS: Load MR1 to enter write leveling mode.
3. diff_DQS is the differential data strobe. Timing reference points are the zero crossings.
4. DQS_t is shown with a solid line; DQS_c is shown with a dotted line.
5. CK_t is shown with a solid dark line; CK_c is shown with a dotted line.
6. DQS needs to fulfill minimum pulse width requirements, tDQSH (MIN) and tDQSL (MIN),
7. as defined for regular WRITEs; the maximum pulse width is system dependent.
8. tWLDQSEN must be satisfied following equation when using ODT:
   - DLL = Enable, then tWLDQSEN > tMOD (MIN) + DODTLon + tADC
   - DLL = Disable, then tWLDQSEN > tMOD (MIN) + tAONAS

Write-Leveling Mode Exit

Write leveling mode should be exited as follows:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note that from this point on, DQ pins are in undefined driving mode and will remain undefined, until tMOD after the respective MR command (Te1).
2. Drive ODT pin LOW (tIS must be satisfied) and continue registering LOW (see Tb0).
3. After RTT is switched off, disable write leveling mode via the MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command can be registered. (MR commands can be issued after tMRD [Td1]).

Write Leveling Exit



Temperature-Controlled Refresh Mode

Normal tREFI Refresh (TCR Disabled)

During normal operation, TCR mode disabled, the DRAM must have a Refresh command issued once every tREFI, except for what is allowed by posting (see Refresh Command section). This means a refresh command must be issued once every 3.9μs if TC greater than or equal to 85°C, and once every 7.8μs if TC less than 85°C as shown in table below.

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc < +45°C	7.8μs	7.8μs	3.9μs [1]	3.9μs [1]
+45°C ≦ Tc < +85°C				
+85°C ≦ Tc < +95°C	NA			

NOTE

1. If Tc is less than 85°C, the external refresh period can be 7.8μs instead of 3.9μs.

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

When TCR mode is enabled, the device will register the externally supplied REFRESH command and adjust the internal refresh period to be longer than tREFI of the normal temperature range, when allowed, by skipping REFRESH commands with the proper gear ratio. TCR mode has two ranges to select between the normal temperature range and the extended temperature range; the correct range must be selected so the internal control operates correctly. The DRAM must have the correct refresh rate applied externally; the internal refresh rate is determined by the DRAM based upon the temperature.

TCR Mode - Normal Temperature Range

REFRESH commands are to be issued to DRAM with the refresh period equal to or shorter than tREFI of normal temperature range (0°C to +85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C. The DRAM may adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when Tc is below 45°C. Not more than three fourths of external refresh commands are skipped at any temperature in this mode. The internal refresh period is automatically adjusted inside the DRAM and the DRAM controller does not need to provide any additional control.

TCR Mode - Extended Temperature Range

REFRESH commands should be issued to DRAM with the refresh period which is tREFI of extended temperature range (+85°C to +95°C). In this mode, the system guarantees that the DRAM temperature does not exceed 95°C. Even though the external Refresh supports the extended temperature range, the DRAM will adjust its internal refresh period to tREFI of the normal temperature range by skipping external REFRESH commands with proper gear ratio when operating in the normal temperature range (0°C to +85°C). The DRAM may furthur adjust the internal refresh period to be longer than tREFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio when Tc is below 45°C. The internal refresh period is automatically adjusted inside the DRAM and the DRAM controller does not need to provide any additional control.

Normal tREFI Refresh (TCR Enabled)

Temperature	Normal Temperature		Extended Temperature	
	External Refresh Period	Internal Refresh Period	External Refresh Period	Internal Refresh Period
Tc < +45°C	7.8μs	> 7.8μs	3.9μs [1]	>> 3.9μs
+45°C ≦ Tc < +85°C		7.8μs		>3.9μs
+85°C ≦ Tc < +95°C	NA			3.9μs

NOTE

1. If the external refresh period is slower than 3.9μs, the device will refresh internally at too slow of a refresh rate and will violate refresh specifications.

Normal temperature mode

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the refresh period equal to or shorter than tREFI of normal temperature range (0°C - 85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.

Below 45°C, DDR4 SDRAM may adjust internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. The internal refresh period adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Extended temperature mode

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the refresh period equal to or shorter than tREFI of extended temperature range (85°C - 95°C).

In the normal temperature range (0°C - 85°C), DDR4 SDRAM adjusts its internal refresh period to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal refresh period to be longer than tREFI of the normal temperature range. The internal refresh period adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

Fine Granularity Refresh Mode

Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device(on-the-fly mode). The on-the-fly mode must be enabled by MRS before any on-the-fly-Refresh command can be issued.

MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	On-the-fly 1x/2x
1	1	0	On-the-fly 1x/4x
1	1	1	Reserved

There are two types of OTF modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two OTF modes is selected (‘A8=1’), DDR4 SDRAM evaluates the BG0 bit when a REFRESH command is issued, and depending on the status of BG0, it dynamically switches its internal refresh configuration between 1x/2x or 1x/4x modes, then executes the corresponding REFRESH operation.

REFRESH Command Truth Table

<table>
<tr><th>Function</th><th>CS_n</th><th>ACT_n</th><th>RAS_n /A15</th><th>CAS_n /A14</th><th>WE_n /A13</th><th>BG1</th><th>BG0</th><th>BA0-1</th><th>A10/ AP</th><th>A0-9, A11-12, A16-20</th><th>MR3[8:6]</th></tr>
<tr><td>Refresh (Fixed rate)</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>V</td><td>V</td><td>V</td><td>V</td><td>V</td><td>A8 = ‘0’</td></tr>
<tr><td>Refresh (on-the-fly 1x)</td><td>L</td><td>H</td><td>L</td><td>L</td><td>H</td><td>V</td><td>L</td><td>V</td><td>V</td><td>V</td><td>A8 = ‘1’</td></tr>
<tr><td>Refresh (on-the-fly 2x)</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">V</td><td rowspan="2">H</td><td rowspan="2">V</td><td rowspan="2">V</td><td rowspan="2">V</td><td>A8:A7:A6=‘101’</td></tr>
<tr><td>Refresh (on-the-fly 4x)</td><td>A8:A7:A6=‘110’</td></tr>
</table>

tREFI and tRFC Parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e., tREFI1 =tREFI(base) (for Tcase<=85°C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values.

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

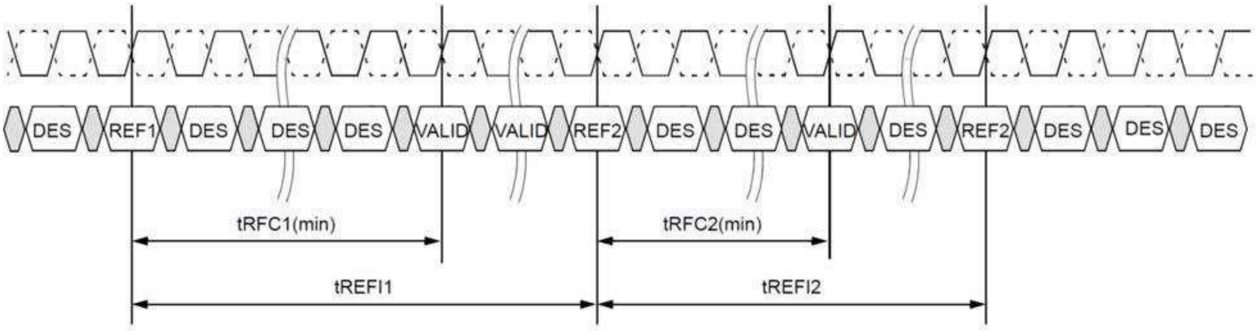
tREFI and tRFC Parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)		7.8	7.8	7.8	7.8	µs
1X mode	tREFI1	0°C <= TCASE <= 85°C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	µs
		85°C < TCASE <= 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	µs
	tRFC1(min)		160	260	350	550	ns
2X mode	tREFI2	0°C <= TCASE <= 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	µs
		85°C < TCASE <= 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	µs
	tRFC2(min)		110	160	260	350	ns
4X mode	tREFI4	0°C <= TCASE <= 85°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	µs
		85°C < TCASE <= 95°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	µs
	tRFC4(min)		90	110	160	260	ns

Changing Refresh Rate

If Refresh rate is changed by either MRS or on-the-fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. When the REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

On-the-fly Refresh Command Timing



The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

1. In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
2. In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
3. In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
4. In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

Usage with Temperature Controlled Refresh Mode

If the temperature controlled refresh mode is enabled, then only the normal mode (fixed 1x mode, MR3 A[8:6] = 000) is allowed. If any other refresh mode than the normal mode is selected, then the temperature controlled refresh mode must be disabled.

Self Refresh Entry and Exit

DDR4 SDRAM can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit.
3. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).
4. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

Multi Purpose Register (MPR)

The multipurpose register (MPR) function, MPR Access Mode, is used to write/read specialized data to/from the DRAM. The MPR consists of four logical Pages, MPR Page 0 through MPR Page 3, with each Page having four 8-bit registers, MPR0 through MPR3.

MPR mode enable and Page selection is done with MRS commands. Data Bus Inversion (DBI) is not allowed during MPR Read operation. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). After MPR is enabled, any subsequent RD or RDA commands will be redirected to a specific mode register.

Once the MPR Access Mode is enabled (MR3 A[2] = 1), only the following commands are allowed: MRS, RD, RDA WR, WRA, DES, REF and Reset; RDA/WRA have the same functionality as RD/WR which means the auto precharge part of RDA/WRA is ignored. The mode register location is specified with the READ command using address bits. The MR is split into upper and lower halves to align with a burst length limitation of 8. Power Down mode and Self-Refresh command are not allowed during MPR enable Mode.

No other command can be issued within tRFC after a REF command has been issued. 1x Refresh is only allowed when MPR mode is Enable. While in MPR Access Mode, MPR read or write sequences must be completed prior to a refresh command.

MR3 Setting for the MPR Access Mode

Address	Operation Mode	Description
A[12:11]	MPR data read format	00 = Serial .... 01 = Parallel 10 = Staggered .... 11 = Reserved
A2	MPR access	0 = Standard operation (MPR not enabled) 1 = MPR data flow enabled
A[1:0]	MPR page selection	00 = Page 0 .... 01 = Page 1 10 = Page 2 .... 11 = Page 3

DRAM Address to MPR UI Translation

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
DRAM address – A*x*	A7	A6	A5	A4	A3	A2	A1	A0
MPR UI – UI*x*	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

MPR Page and MPRx Definitions

MPR Page 0 – Read or Write (Data Patterns)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="4">BA1:BA0</td><td>00 = MPR0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td rowspan="4">Read/Write (default value)</td></tr>
<tr><td>01= MPR1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>10 = MPR2</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>11 = MPR3</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

MPR Page 1 – Read-only (CA Parity Error Log)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="5">BA1:BA0</td><td>00 = MPR0</td><td>A[7]</td><td>A[6]</td><td>A[5]</td><td>A[4]</td><td>A[3]</td><td>A[2]</td><td>A[1]</td><td>A[0]</td><td rowspan="5">Read-only</td></tr>
<tr><td>01 = MPR1</td><td>CAS_n/ A15</td><td>WE_n/ A14</td><td>A[13]</td><td>A[12]</td><td>A[11]</td><td>A[10]</td><td>A[9]</td><td>A[8]</td></tr>
<tr><td>10 = MPR2</td><td>PAR</td><td>ACT_n</td><td>BG[1]</td><td>BG[0]</td><td>BA[1]</td><td>BA[0]</td><td>A[17]</td><td>RAS_n/ A16</td></tr>
<tr><td rowspan="2">11 = MPR3</td><td rowspan="2">CRC Error Status</td><td rowspan="2">CA Parity Error Status</td><td colspan="3">CA Parity Latency</td><td rowspan="2">C[2]</td><td rowspan="2">C[1]</td><td rowspan="2">C[0]</td></tr>
<tr><td>MR5.A[2]</td><td>MR5.A[1]</td><td>MR5.A[0]</td></tr>
</table>

MPR Page 2 – Read-only (MRS Readout)

<table>
<tr><th>Address</th><th>MPR Location</th><th>[7]</th><th>[6]</th><th>[5]</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>note</th></tr>
<tr><td rowspan="12">BA1:BA0</td><td rowspan="3">00 = MPR0</td><td>RFU</td><td>RFU</td><td>RFU</td><td colspan="2">Temperature Sensor Status</td><td>CRC Write Enable</td><td colspan="2">RTT_WR</td><td rowspan="12">Read-only</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>MR2</td><td colspan="2">MR2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>A12</td><td>A10</td><td>A9</td></tr>
<tr><td rowspan="3">01= MPR1</td><td>VREFDQ Training Range</td><td colspan="6">VREFDQ Training Value</td><td>Gear-down Enable</td></tr>
<tr><td>MR6</td><td colspan="6">MR6</td><td></td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>A3</td></tr>
<tr><td rowspan="3">10 = MPR2</td><td colspan="4">CAS Latency</td><td>RFU</td><td colspan="3">CAS Write Latency</td></tr>
<tr><td colspan="4">MR0</td><td>-</td><td colspan="3">MR2</td></tr>
<tr><td>A6</td><td>A5</td><td>A4</td><td>A2</td><td>-</td><td>A5</td><td>A4</td><td>A3</td></tr>
<tr><td rowspan="3">11 = MPR3</td><td colspan="3">RTT_WR</td><td colspan="3">RTT_Park</td><td colspan="2">Driver Impedance</td></tr>
<tr><td colspan="3">MR1</td><td colspan="3">MR5</td><td colspan="2">MR2</td></tr>
<tr><td>A10</td><td>A9</td><td>A6</td><td>A8</td><td>A7</td><td>A6</td><td>A2</td><td>A1</td></tr>
</table>

MPR Page 3 – Read-only (Vendor Purpose Only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care								Read-only
	01= MPR1	don't care								
	10 = MPR2	don't care								
	11 = MPR3	don't care								

MPR Reads

MPR reads are supported using BL8 and BC4 modes. Burst length on-the-fly is not supported for MPR reads. Data bus inversion (DBI) is not allowed during MPR READ operation; the device will ignore the Read DBI enable setting in MR5 [12] when in MPR mode. READ commands for BC4 are supported with a starting column address of A[2:0] = 000 or 100. After power-up, the content of MPR Page 0 has the default values. MPR page 0 can be rewritten via an MPR WRITE command. The device maintains the default values unless it is rewritten by the DRAM controller. If the DRAM controller does overwrite the default values (Page 0 only), the device will maintain the new values unless re-initialized or there is power loss.

Timing in MPR mode:

- Reads (back-to-back) from Page 0 may use tCCD_S or tCCD_L timing between READ commands
- Reads (back-to-back) from Pages 1, 2, or 3 may not use tCCD_S timing between READ commands; tCCD_L must be used for timing between READ commands

The following steps are required to use the MPR to read out the contents of a mode register (MPR Page x, MPRy).

1. The DLL must be locked if enabled.
2. Precharge all; wait until tRP is satisfied.
3. MRS command to MR3[2] = 1 (Enable MPR data flow), MR3[12:11] = MPR read format, and MR3[1:0] MPR page.
   a. MR3[12:11] MPR read format:
      1. 00 = Serial read format
      2. 01 = Parallel read format
      3. 10 = staggered read format
      4. 11 = RFU
   b. MR3[1:0] MPR page:
      1. 00 = MPR Page 0
      2. 01 = MPR Page 1
      3. 10 = MPR Page 2
      4. 11 = MPR Page 3
4. tMRD and tMOD must be satisfied.
5. Redirect all subsequent READ commands to specific MPRx location.
6. Issue RD or RDA command.
   a. BA1 and BA0 indicate MPRx location:
      1. 00 = MPR0
      2. 01 = MPR1
      3. 10 = MPR2

    4. 11 = MPR3

  b. A12/BC = 0 or 1; BL8 or BC4 fixed-only, BC4 OTF not supported.

    1. If BL = 8 and MR0 A[1:0] = 01, A12/BC must be set to 1 during MPR READ commands.

  c. A2 = burst-type dependant:

    1. BL8: A2 = 0 with burst order fixed at 0, 1, 2, 3, 4, 5, 6, 7
    2. BL8: A2 = 1 not allowed
    3. BC4: A2 = 0 with burst order fixed at 0, 1, 2, 3, T, T, T, T
    4. BC4: A2 = 1 with burst order fixed at 4, 5, 6, 7, T, T, T, T

  d. A[1:0] = 00, data burst is fixed nibble start at 00.

  e. Remaining address inputs, including A10, and BG1 and BG0 are "Don't Care."

7. After RL = AL + CL, DRAM bursts data from MPRx location; MPR readout format determined by MR3[A12,11,1,0].
8. Steps 5 through 7 may be repeated to read additional MPRx locations.
9. After the last MPRx READ burst, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3[2] = 0.
11. After the tMOD sequence is completed, the DRAM is ready for normal operation from the core (such as ACT).

MPR Readout Format

The MPR read data format can be set to three different settings: serial, parallel, and staggered.

MPR Readout Serial Format

The serial format is required when enabling the MPR function to read out the contents of an MRx, temperature sensor status, and the command address parity error frame. However, data bus calibration locations (four 8-bit registers) can be programmed to read out any of the three formats. The DRAM is required to drive associated strobes with the read data similar to normal operation (such as using MRS preamble settings).

Serial format implies that the same pattern is returned on all DQ lanes, as shown the table below, which uses values programmed into the MPR via [7:0] as 0111 1111.

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

MPR Readout Parallel Format

Parallel format implies that the MPR data is returned in the first data UI and then repeated in the remaining UIs of the burst, as shown in the table below. Data pattern location 0 is the only location used for the parallel format. RD/RDA from data pattern locations 1, 2, and 3 are not allowed with parallel data return mode. In this example, the pattern programmed in the data pattern location 0 is 0111 1111. The x4 configuration only outputs the first four bits (0111 in this example). For the x16 configuration, the same pattern is repeated on both the upper and lower bytes.

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

MPR Readout Staggered Format

Staggered format of data return is defined as the staggering of the MPR data across the lanes. In this mode, an RD/RDA command is issued to a specific data pattern location and then the data is returned on the DQ from each of the different data pattern locations.

For the x4 configuration, an RD/RDA to data pattern location 0 will result in data from location 0 being driven on DQ0, data from location 1 being driven on DQ1, data from location 2 being driven on DQ2, and so on. Similarly, an RD/RDA command to data pattern location 1 will result in data from location 1 being driven on DQ0, data from location 2 being driven on DQ1, data from location 3 being driven on DQ2, and so on.

MPR Readout Staggered Format, x4

READ MPR0 Command		READ MPR1 Command		READ MPR2 Command		READ MPR3 Command	
Stagger	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**
DQ0	MPR0	DQ0	MPR1	DQ0	MPR2	DQ0	MPR3
DQ1	MPR1	DQ1	MPR2	DQ1	MPR3	DQ1	MPR0
DQ2	MPR2	DQ2	MPR3	DQ2	MPR0	DQ2	MPR1
DQ3	MPR3	DQ3	MPR0	DQ3	MPR1	DQ3	MPR2

It is expected that the DRAM can respond to back-to-back RD/RDA commands to the MPR for all DDR4 frequencies so that a sequence (such as the one that follows) can be created on the data bus with no bubbles or clocks between read data. In this case, the system memory controller issues a sequence of RD(MPR0), RD(MPR1), RD(MPR2),RD(MPR3), RD(MPR0), RD(MPR1), RD(MPR2), and RD(MPR3).

MPR Readout Staggered Format, x4 – Consecutive READs

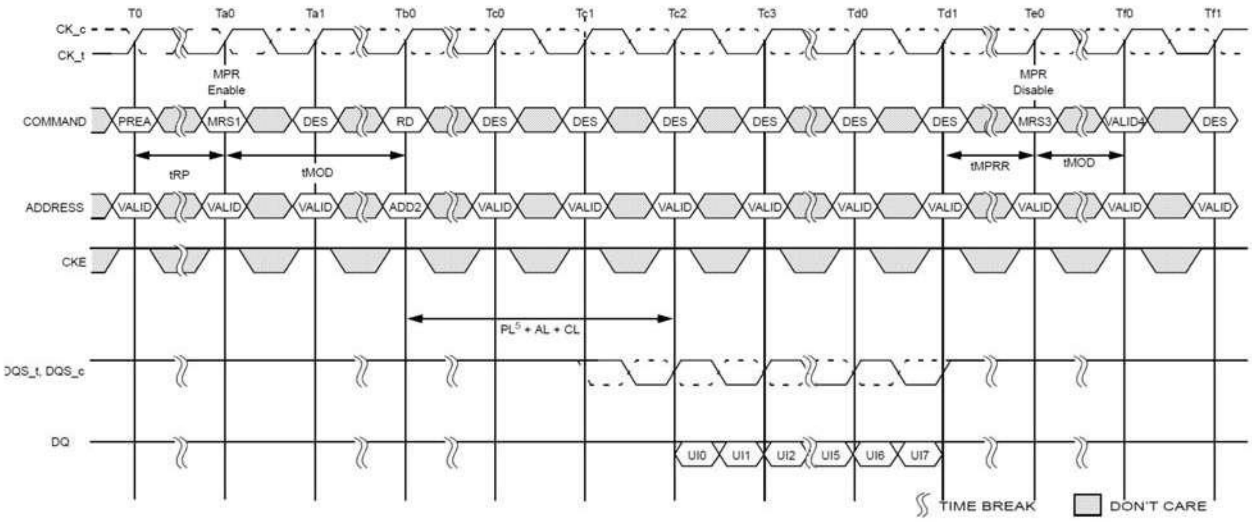
Stagger	UI[7:0]	UI[15:8]	UI[23:16]	UI[31:24]	UI[39:32]	UI[47:40]	UI[55:48]	UI[63:56]
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

For the x8 configuration, the same pattern is repeated on the lower nibble as on the upper nibble. READs to other MPR data pattern locations follow the same format as the x4 case.

MPR Readout Staggered Format, x8 and x16

x8 READ MPR0 Command		x16 READ MPR0 Command		x16 READ MPR0 Command	
Stagger	**UI[7:0]**	**Stagger**	**UI[7:0]**	**Stagger**	**UI[7:0]**
DQ0	MPR0	DQ0	MPR0	DQ8	MPR0
DQ1	MPR1	DQ1	MPR1	DQ9	MPR1
DQ2	MPR2	DQ2	MPR2	DQ10	MPR2
DQ3	MPR3	DQ3	MPR3	DQ11	MPR3
DQ4	MPR0	DQ4	MPR0	DQ12	MPR0
DQ5	MPR1	DQ5	MPR1	DQ13	MPR1
DQ6	MPR2	DQ6	MPR2	DQ14	MPR2
DQ7	MPR3	DQ7	MPR3	DQ15	MPR3

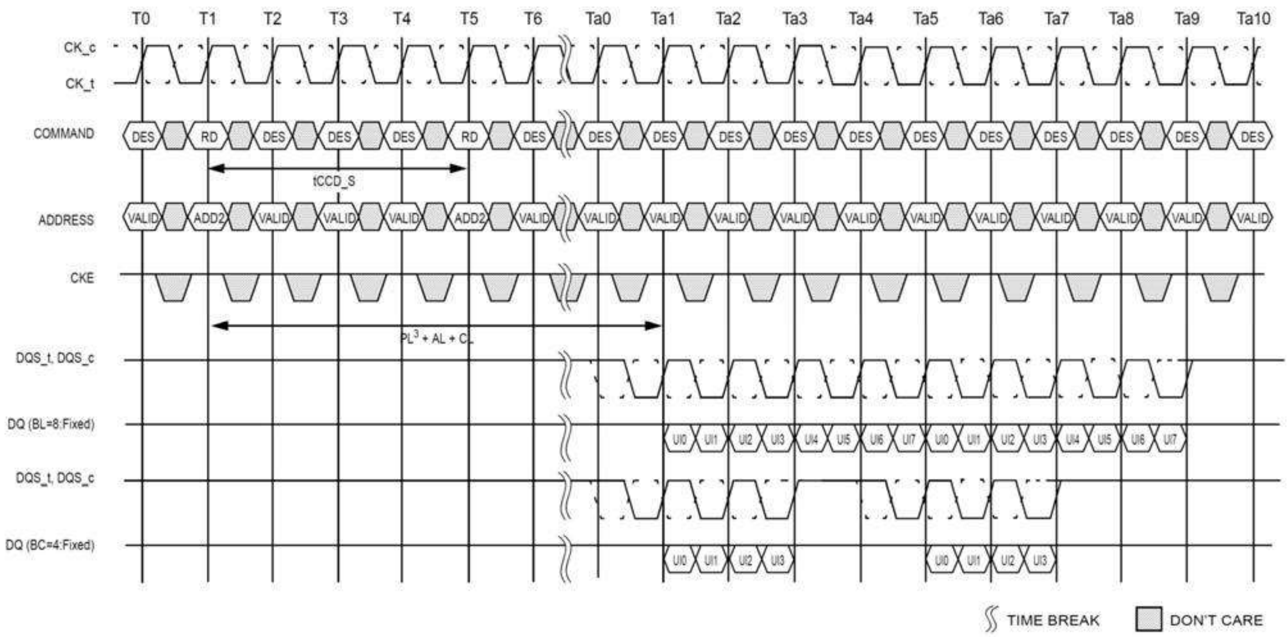
MPR READ Timing



NOTE

1. Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent readsand writes to MPR locations.
2. Address setting:
   - A[1:0] = “00”(data burst order is fixed starting at nibble, always 00b here)
   - A[2]= 0(For BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are "Don’t Care" including BG1 and BG0.
   - A12 is don’t carewhen MR0 A[1:0] = 00 or 10, and must be “1”when MR0 A[1:0] = 01
3. Multipurpose registers Read/Write Disable (MR3 A2 = 0).
4. Continue with regular DRAM command.
5. Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR Back-to-Back READ Timing



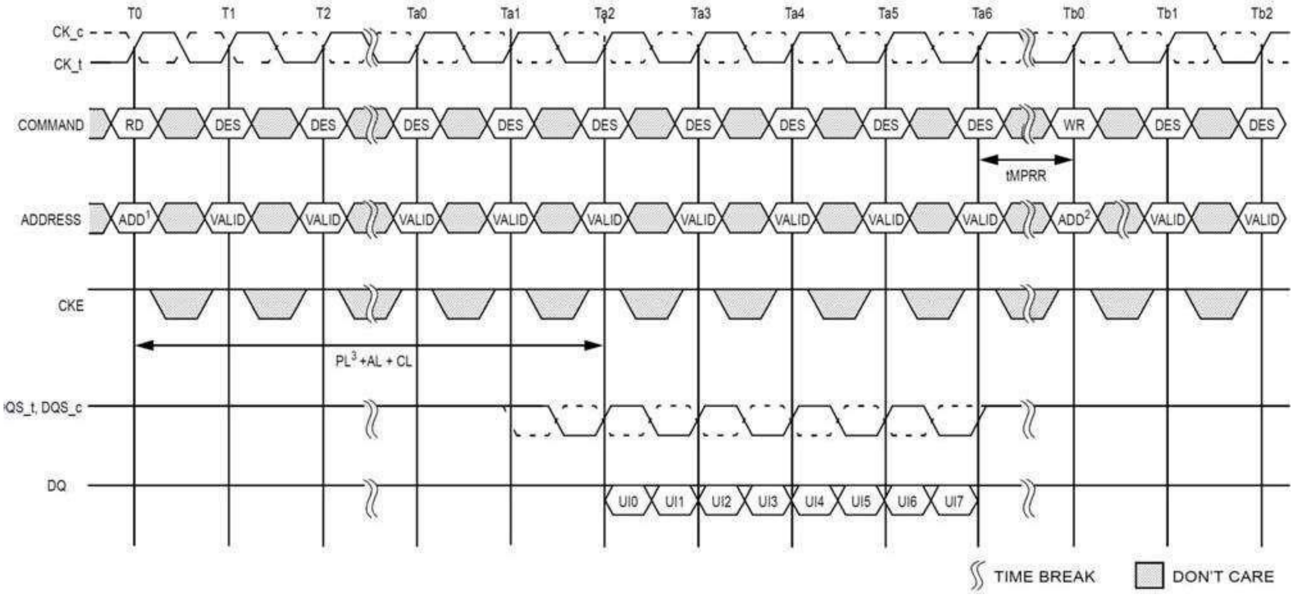
NOTE

1. tCCD_S = 4, Read Preamble = 1tCK
2. Address setting:
   - A[1:0] = 00(data burst order is fixed starting at nibble, always 00b here)
   - A[2] = 0(for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7; for BC = 4, burst order isfixed at 0, 1, 2, 3, T, T, T, T)

- BA1 and BA0 indicate the MPR location
- A10 and other address pins are "Don't Care" including BG1 and BG0.
- A12 is "Don'tCare" when MR0 A[1:0] = 00 or 10, and must be "1"when MR0 A[1:0] = 01

3. Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR READ-to-WRITE Timing



NOTE

1. Address setting:
   - A[1:0] = 00(data burst order is fixed startingat nibble, always 00 here)
   - A[2]= 0(for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are "Don't Care" including BG1 and BG0.
   - A12 is"Don'tCare" when MR0 A[1:0] = 00, and must be 1b when MR0 A[1:0] = 01
2. Address setting:
   - BA1 and BA0 indicate the MPR location
   - A [7:0] = data for MPRA10 and other address pins are don't care.
3. Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

MPR Writes

MPR Access Mode allows 8-bit writes to the MPR location using the address bus A7:A0(refer to table: DRAM Address to MPR UI 8-bit Registers Translation)

The following steps are required to use the MPR to write to mode register MPR Page 0.

1. The DLL must be locked prior to MPR Writes. DLL is Enabled, MR1 A0 = 1
2. Precharge all; wait until tRP is satisfied.
3. MR3 A2 = 1 (Enable MPR data flow) and MR3 A[1:0] = 00 (MPR Page 0); 01, 10, 11 = Not allowed.
4. Redirect all subsequent Write commands to specific MPR location.
5. tMRD and tMOD must be satisfied.
6. Issue WR or WRA command:

   a. BA1 and BA0 indicate MPR location:

   00 = MPR0

   01 = MPR1

   10 = MPR2

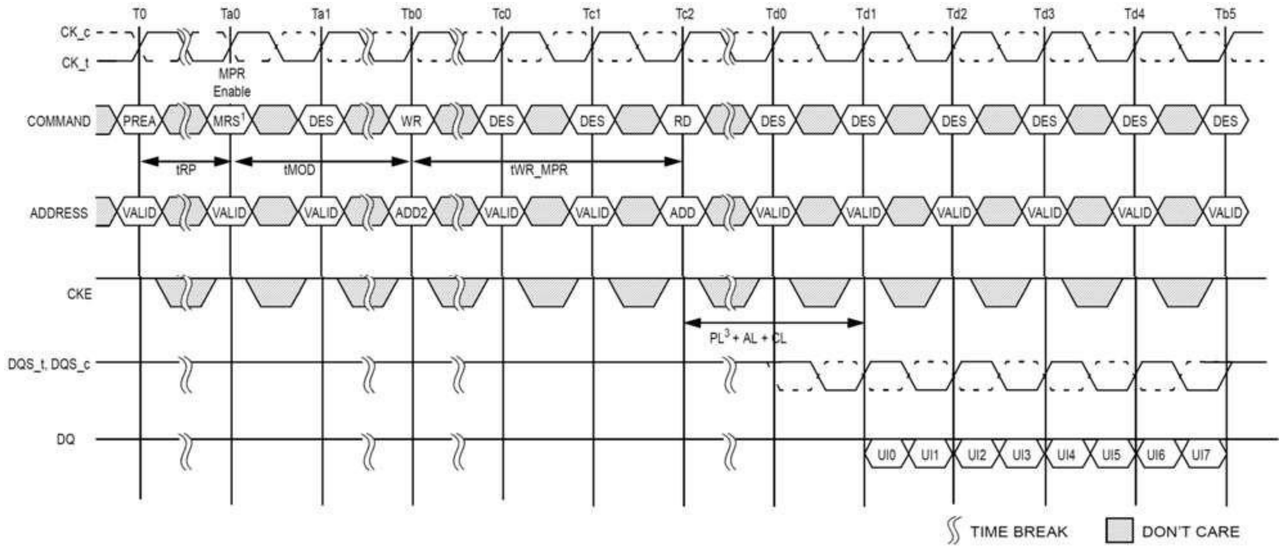
   11 = MPR3

b. A[7:0] = data for MPR Page 0, mapped A[7:0] to UI[0:7] .

c. Remaining address inputs, including A10, BG0 and BG1 are don't care.

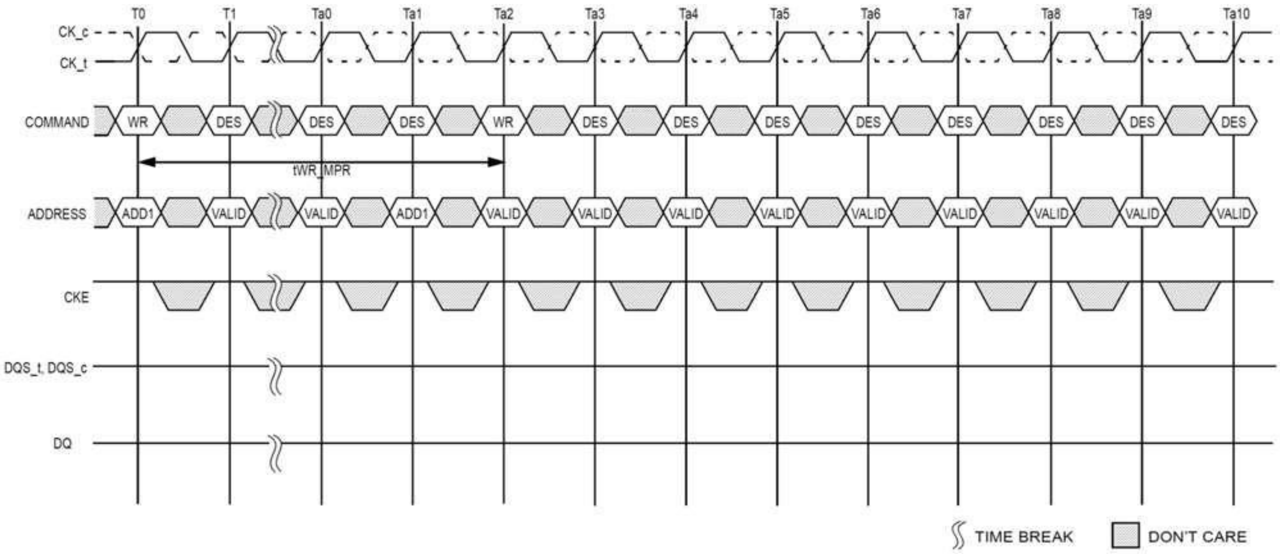
7. tWR_MPR must be satisfied to complete MPR Write.
8. Steps 5 through 7 may be repeated these calibration writes and reads until data capture at memory controller is optimized.
9. After the last MPR location Write, tMPRR must be satisfied prior to exiting.
10. Issue MRS command to exit MPR mode; MR3 A2= 0.
11. Wait until tMRD and tMOD are satisfied; Continue with regular DRAM commands like Activate.

MPR WRITE and WRITE-to-READ Timing



NOTE
1. Multipurpose registers Read/Write Enable (MR3 A2 = 1).
2. Address setting:
   - BA1 and BA0 indicate the MPR location
   - A [7:0] = data for MPR
   - A10 and other address pins are "Don't Care"
3. Parity latency (PL) is added to data output delay when C/A parity latency mode is enabled.

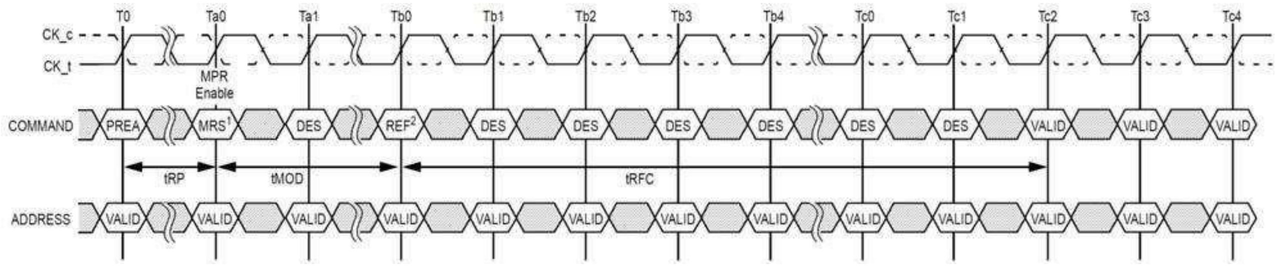
MPR Back-to-Back WRITE Timing



NOTE

1. Address setting:
   - BA1 and BA0 indicate the MPR location
   - A [7:0] = data for MPR
   - A10 and other address pins are "Don't Care"

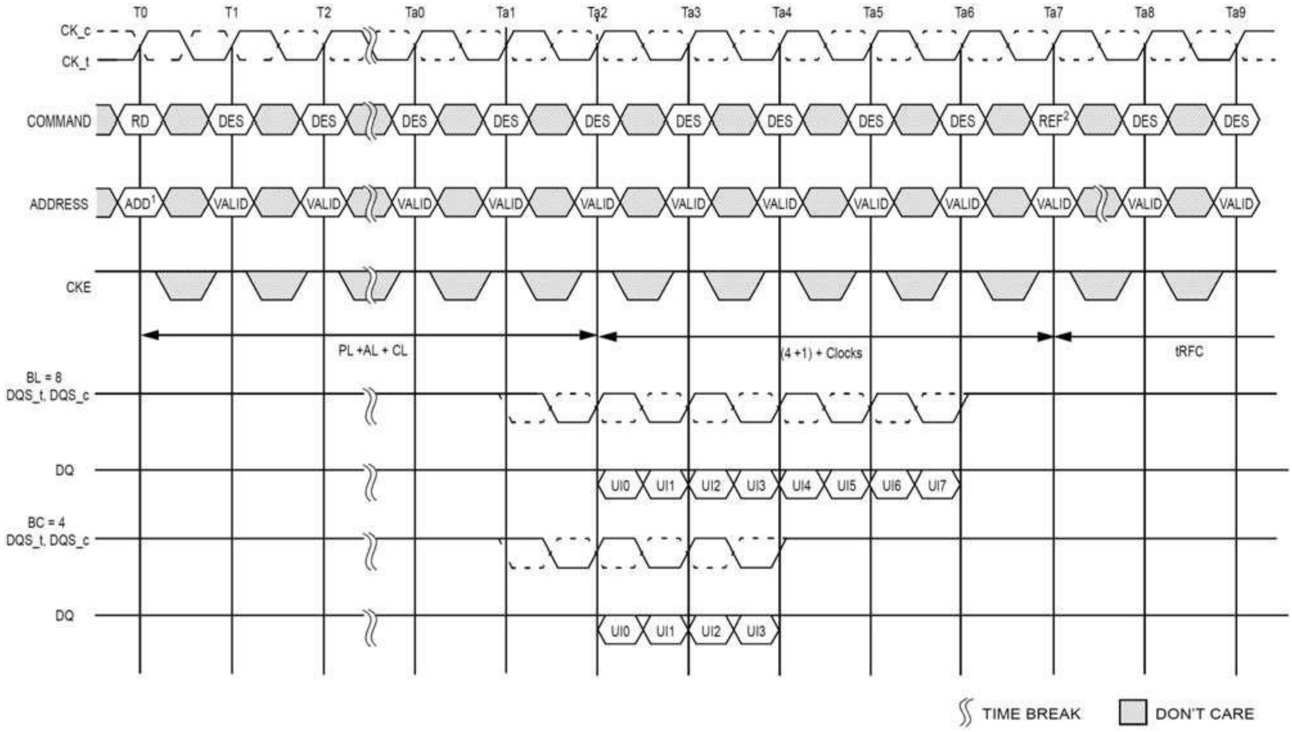
REFRESH Command Timing



NOTE

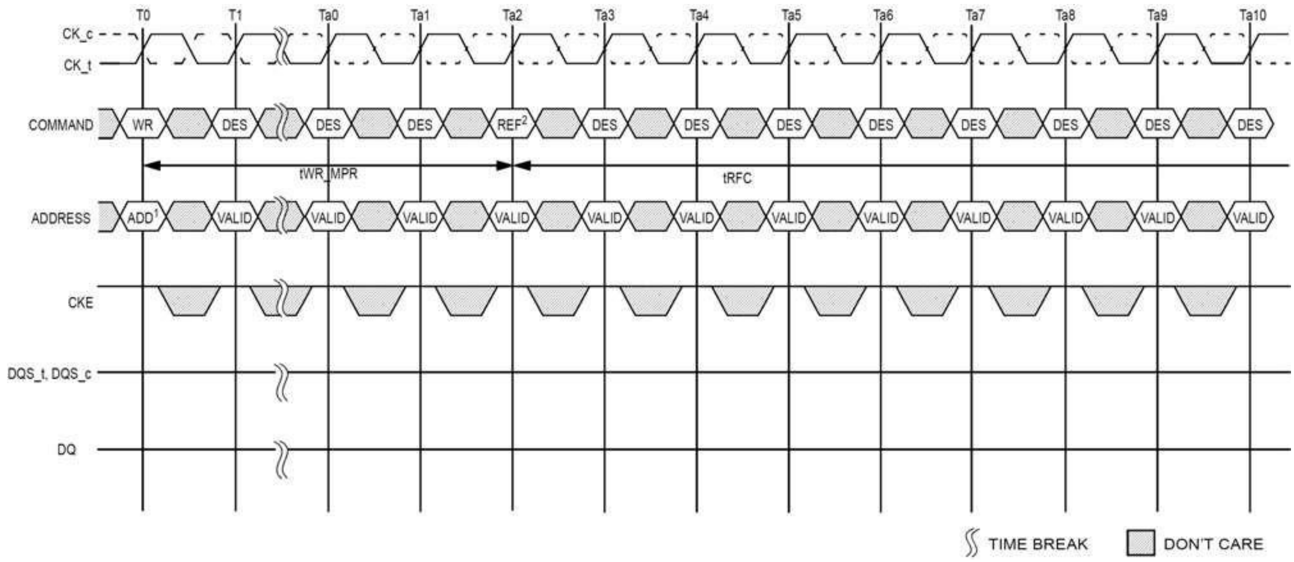
1. Multipurpose registers Read/Write Enable (MR3 A2 = 1). Redirect all subsequent readand writes to MPR locations.
2. 1x refresh is only allowed when MPR mode is enabled.

READ-to-REFRESH Command Timing



NOTE
1. Address setting:
   - A[1:0] = 00(data burst order is fixedstarting at nibble, always 00 here)
   - A[2]= 0 (for BL = 8, burst order is fixed at 0, 1, 2, 3, 4, 5, 6, 7)
   - BA1 and BA0 indicate the MPR location
   - A10 and other address pins are "Don't Care" including BG1 and BG0.
   - A12 is "Don'tCare" when MR0 A[1:0] = 00 or 10, and must be 1b when MR0 A[1:0] = 01
2. 1x refresh is only allowed when MPR mode is enabled.

WRITE-to-REFRESH Timing



NOTE
1. Address setting:
   - BA1 and BA0 indicate the MPR location; - A [7:0] = data for MPR; - A10 and other address pins are "Don't Care"
2. 1x refresh is only allowed when MPR mode is enabled.

Data Mask(DM), Data Bus Inversion (DBI) and TDQS

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) functionon in x8 and x16 DRAM configuration. x4 DDR4 SDRAM does not support DM and DBI function. x8 DDR4 SDRAM supports TDQS function. x4 and x16 DDR4 SDRAM does not support TDQS function.

DM, DBI & TDQS functions are supported with dedicated one pin labeled as DM_n/DBI_n/TDQS_t. The pin is bi-directional pin for DRAM. The DM_n/DBI _n pin is Active Low as DDR4 supports VDDQ reference termination. TDQS function does not drive actual level on the pin.

DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A11 in MR1 and bit A12:A10 in MR5.

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultanteously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.

Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM and DBI functions are supported. When TDQS function is enabled, the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins.

DBI vs. DM vs. TDQS Function Matrix

Read DBI	Write DBI	Data Mask (DM)	TDQS (x8 only)
Enabled (or Disabled) **MR5[12]=1** (or MR5[12] = 0)	Disabled MR5[11] = 0	Disabled MR5[10] = 0	Disabled MR1[11] = 0
	Enabled MR5[11] = 1	Disabled MR5[10] = 0	Disabled MR1[11] = 0
	Disabled MR5[11] = 0	**Enabled** MR5[10] = 1	Disabled MR1[11] = 0
Disabled MR5[12] = 0	Disabled MR5[11] = 0	Disabled MR5[10] = 0	**Enabled** MR1[11] = 1

DM function during Write operation: DRAM masks the write data received on the DQ inputs if DM_n was sampled Low on a given byte lane. If DM_n was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if DBI_n was sampled Low on a given byte lane. If DBI_n was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives DBI_n pin Low when the number of ‘0’ data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives DBI_n pin High.

x8 DRAM Write DQ Frame Format

Function	Data transfer							
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DM_n or DBI_n	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

x8 DRAM Read DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DBI_n	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

x16 DRAM Write DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DML0 or DBIL0	DML1 or DBIL1	DML2 or DBIL2	DML3 or DBIL3	DML4 or DBIL4	DML5 or DBIL5	DML6 or DBIL6	DML7 or DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBIU_n	DMU0 or DBIU0	DMU1 or DBIU1	DMU2 or DBIU2	DMU3 or DBIU3	DMU4 or DBIU4	DMU5 or DBIU5	DMU6 or DBIU6	DMU7 or DBIU7

x16 DRAM Read DQ Frame Format

Function	Data transfer							
	0	1	2	3	4	5	6	7
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DBIL_n	DBIL0	DBIL1	DBIL2	DBIL3	DBIL4	DBIL5	DBIL6	DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DBIU_n	DBIU0	DBIU1	DBIU2	DBIU3	DBIU4	DBIU5	DBIU6	DBIU7

ZQ Calibration Commands

ZQ Calibration command is used to calibrate DRAM RON and ODT values. The device needs a longer time to calibrate the output driver and on-die termination circuits at initialization and a relatively smaller time to perform periodic calibrations.

The ZQCL command is used to perform the initial calibration during the power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which is reflected as an updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

The ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ correction) of RON and R_{TT} impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the Output Driver and ODT Voltage and Temperature Sensitivity tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the device is subjected to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQ\ \text{correction}}{(T\text{sense} \times T\text{drift rate}) + (V\text{sense} \times V\text{drift rate})}$$

where Tsense = max(dRTTdT, dRONdTM) and Vsense = max(dRTTdV, dRONdVM) define the temperature and voltage sensitivities.

For example, if Tsense = 1.5% / °C, Vsense = 0.15% / mV, Tdrift_rate = 1°C / sec and Vdrift_rate = 15 mV /sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

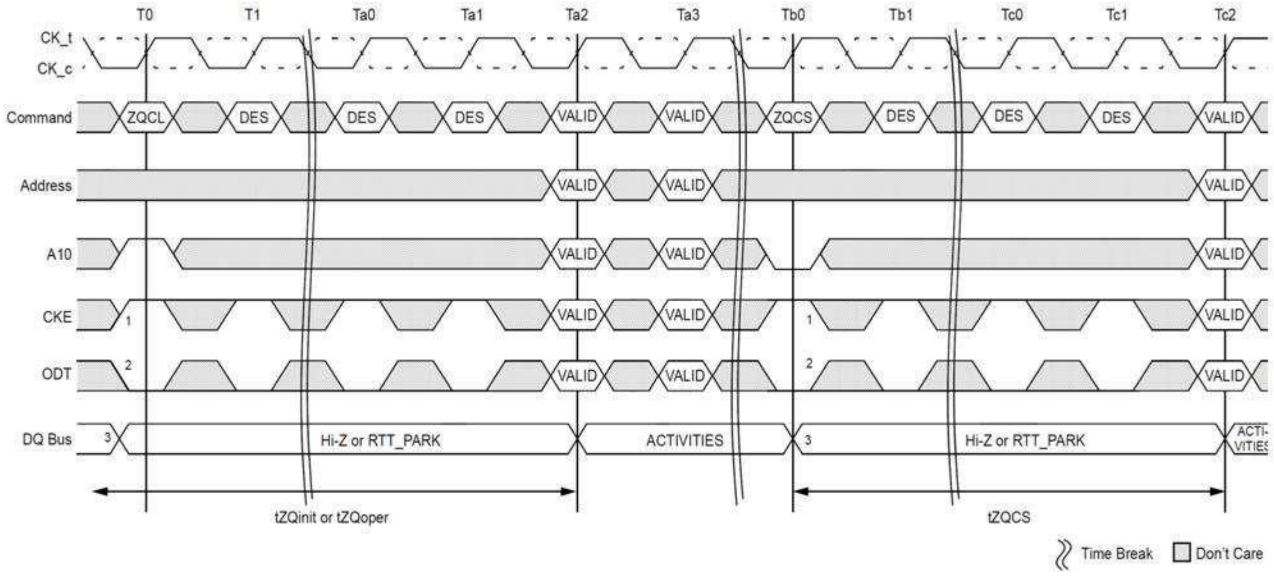
No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the device should disable the ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon self refresh exit, the device will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for a ZQ calibration command (short or long) after self refresh exit is XS, XS_Abort/ XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.

ZQ Calibration Timing



NOTE

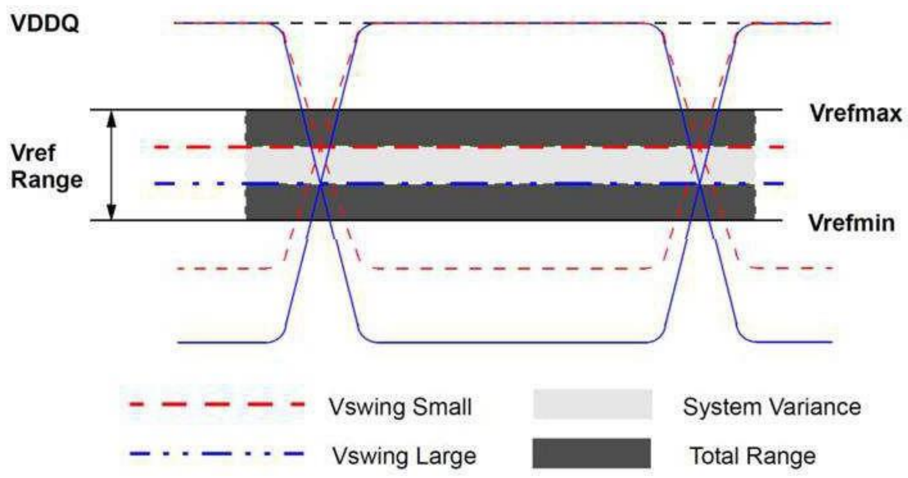
1. CKE must be continuously registered HIGH during the calibration procedure.
2. During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide R_{TT_PARK}.
3. All devices connected to the DQ bus should be High Z or R_{TT_PARK} during the calibration procedure.

DQ VREF Training

The DRAM internal DQ VREF specification parameters are operating voltage range, stepsize, VREF step time, VREF full step time and VREF valid level.

The voltage operating range specifies the minimum required VREF setting range for DDR4 DRAM devices. The minimum range is defined by VREFmax and VREFmin as depicted in the following figure.

VREF operating range (VREFmin, VREFmax)

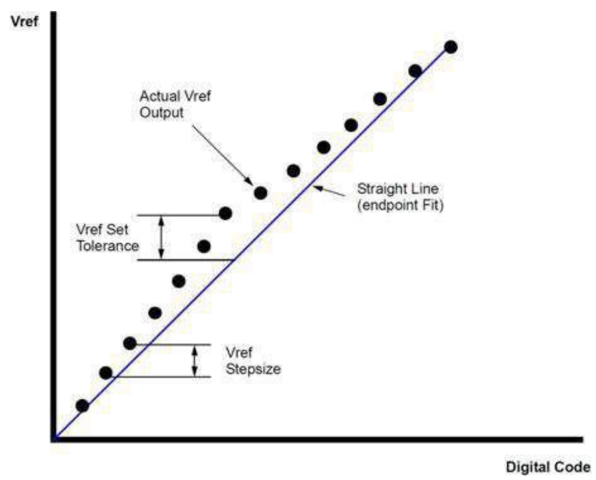


The VREF stepsize is defined as the stepsize between adjacent steps. VREF stepsize ranges from 0.5% VDDQ to 0.8% VDDQ.However, for a given design, DRAM has one value for VREF step size that falls within the range.

The VREF set tolerance is the variation in the VREF voltage from the ideal setting. This accounts for accumulated error over multiplesteps. There are two ranges for VREF set tolerance uncertainity. The range of VREF set tolerance uncertainty is a function of number of steps n.

The VREF set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max VREF values for a specified range. An illustration depicting an example of the stepsize and VREF set tolerance is below.

Example of VREF Set Tolerance and Step Size



The VREF increment/decrement step times are defined by VREF_time. VREF_time is defined from t0 to t1, where t1 is referenced to when the VREF voltage is at the final DC level within the VREF valid tolerance (VREF_val_tol).

The VREF valid level is defined by VREF_val tolerance to qualify the step time t1. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any VREF increment/decrement adjustment.

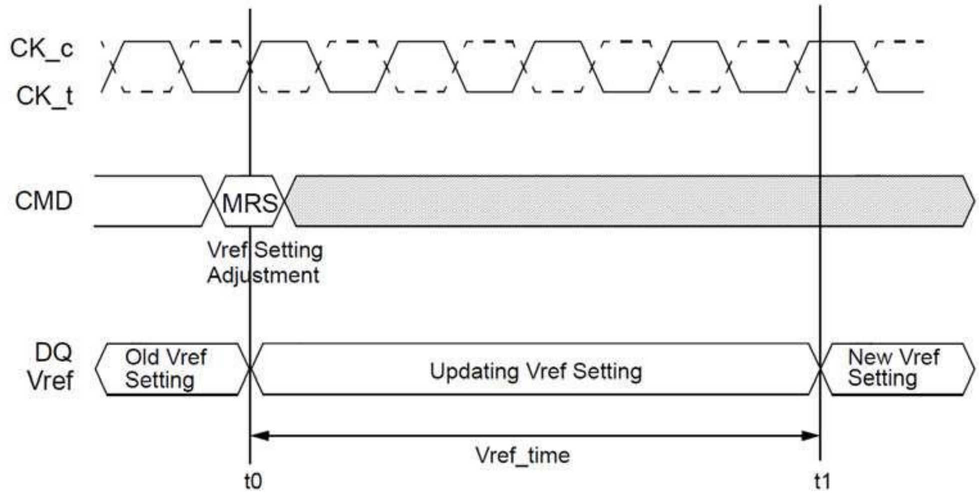
This parameter is only applicable for DRAM component level validation/charachterization.

VREF_time is the time including up to VREF,min to VREF,max or VREF,max to VREF,min change in VREF voltage.

t0 - is referenced to MRS command clock

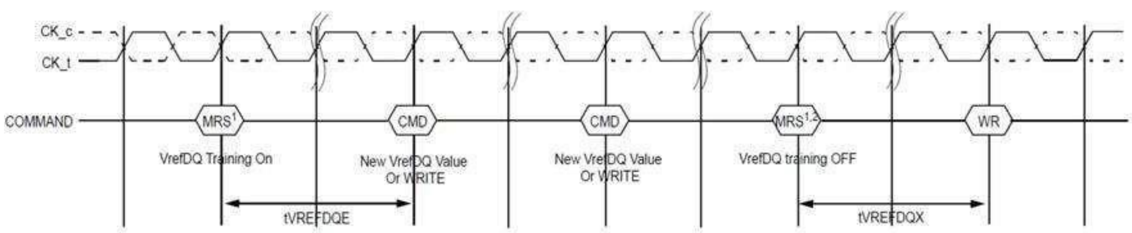
t1 - is referenced to the VREF_val_tol

VREF_time for short and long timing diagram



A MRS command to the mode register bits 5:0 of MR6 are used to program the vref value. VREFDQ training mode is enabled/disabled by A7 of MR6 and training range can be selected by A6 of MR6. When VREFDQ training mode is entered/exited, the following parameter needs to be satisfied to prevent current consumption and also stable operation.

VREFDQ Training Mode Entry and Exit Timing Diagram



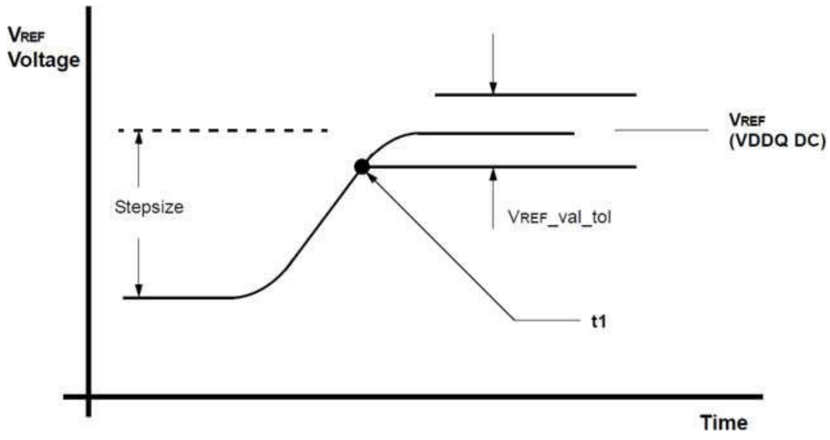
NOTE

1. The MR command used to enter VrefDQ Calibration Mode treats MR6 a[5:0] as don' t care while thenext subsequent MR command sets VrefDQ values in MR6 A[5:0]
2. Depending on the step size of the latest programmed VREF value, Vref_timemust be satisfied before disabling VrefDQ training mode.

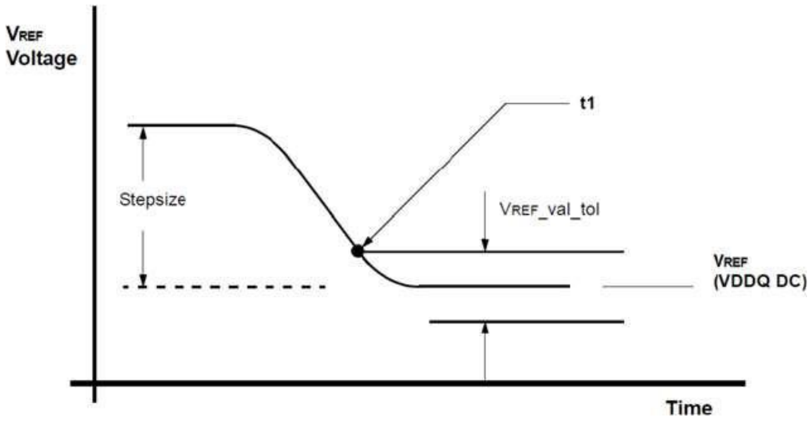
AC Parameters of DDR4 VREFDQ Training

Speed		DDR4-1600,1866,2133,2400,2666, 2933,3200		Unit	NOTE
Parameter	Symbol	MIN	MAX		
VREFDQ training					
Enter VrefDQ training mode to the first write or VREFDQ MRS command delay	tVREFDQE	150	-	ns	
Exit VrefDQ training mode to the first write command delay	tVREFDQX	150	-	ns	

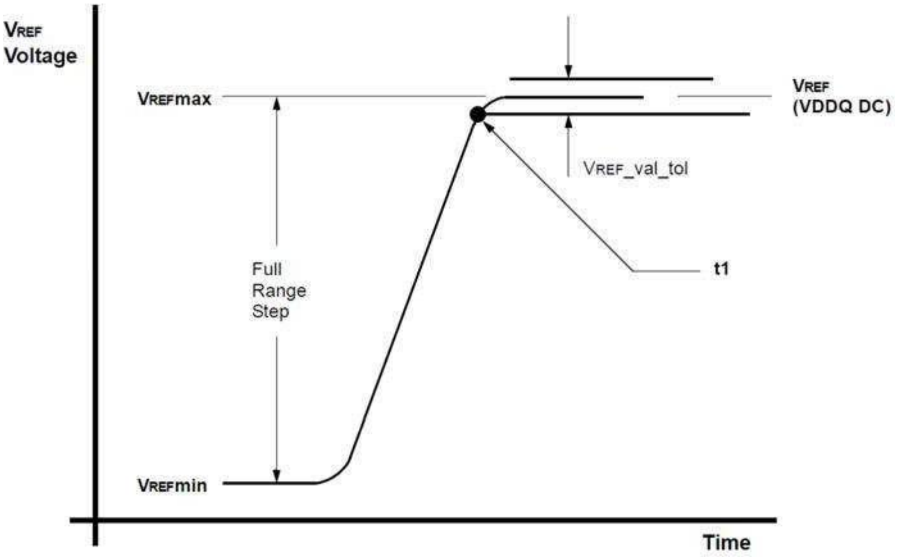
VREF step single stepsize increment case



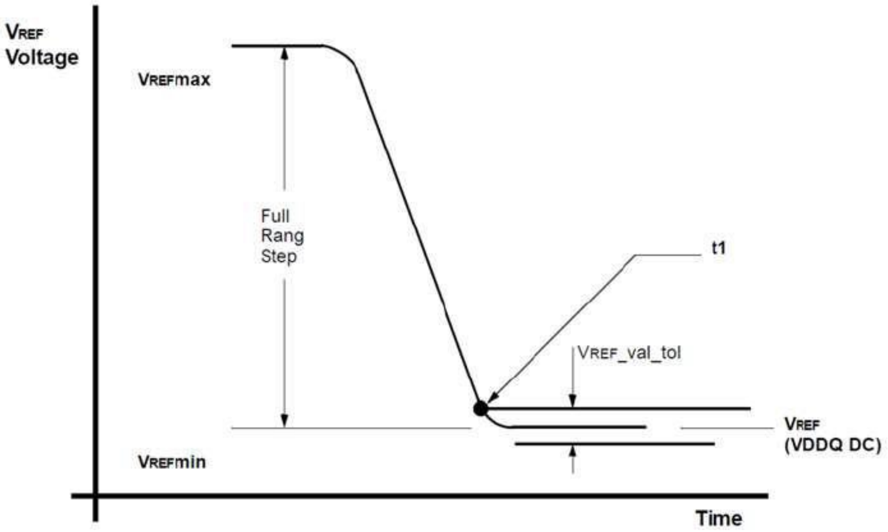
VREF step single stepsize decrement case



VREF full step from VREFmin to VREFmax case



VREF full step from VREFmax to VREFmin case



VREFDQ Supply and Calibration Ranges

The DDR4 SDRAM internally generates its own VREFDQ. DRAM internal VREFDQ specification parameters: voltage range, step-size, VREF step time, VREF full step time, and VREF valid level. The voltage operating range specifies the minimum required VREF setting range for DDR4 DRAM devices. The minimum range is defined by VREFDQ,min and VREFDQ,max. A calibration sequence should be performed by the DRAM controller to adjust VREFDQ and optimize the timing and voltage margin of the DRAM data input receivers.

VREFDQ Specification

Prarmeter	Symbol	Min	Typ	Max	Unit	NOTE
VREF operating point Range1	VREFDQ R1	60%	-	92%	VDDQ	1, 11
VREF operating point Range2	VREFDQ R2	45%	-	77%	VDDQ	1, 11
VREF Stepsize	VREF,step	0.50%	0.65%	0.80%	VDDQ	2
VREF Set Tolerance	VREF,set_tol	-1.625%	0.00%	1.625%	VDDQ	3,4,6
		-0.15%	0.00%	0.15%	VDDQ	3,5,7
VREF Step Time	VREF,time	-	-	150	ns	8,9,12
VREF Valid tolerance	VREF_val_tol	-0.15%	0.00%	0.15%	VDDQ	10

NOTE
1. VREF (DC) voltage is referenced to VDDQ(DC). VDDQ(DC) is 1.2V.
2. VREF step size increment/decrement range. VREF at DC level.
3. VREF_new = VREF_old ± n × VREF_step; n = number of steps. If increment, use "+;" if decrement, use "-".
4. The minimum value of VREF setting tolerance = VREF_new -1.625% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 1.625% × VDDQ for n>4.
5. The minimum value of VREF setting tolerance = VREF_new -0.15% × VDDQ. The maximum value of VREF setting tolerance = VREF_new + 0.15% × VDDQ for n>4.
6. Measured by recording the MIN and MAX values of the VREF output over the range, drawing a straight line between those points, and comparing all other VREF output settings to that line.
7. Measured by recording the MIN and MAX values of the VREF output across four consecutive steps (n = 4), drawing a straight line between those points, and comparing al VREF output settings to that line.
8. Time from MRS command to increment or decrement one step size for VREF.
9. Time from MRS command to increment or decrement one step size up to the full range of VREF.
10. Only applicable for DRAM component-level test/characterization purposes. Not applicable for normal mode of operation. VREF valid qualifies the step times, which will be characterized at the component level.
11. DRAM range 1 or range 2 is set by the MRS bit, MR6 A6.
12. If the VREF monitor is enabled, VREF_time must be derated by: +10ns if DQ bus load is 0pF and anadditional +15ns/pF of DQ bus loading.

Per-DRAM Addressability (PDA Mode)

DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank.

1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.
   - RTT_PARK MR5 {A8:A6} = Enable
   - RTT_NOM MR1 {A10:A9:A8} = Enable
3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1".
4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0. DRAM captures DQ0 by using DQS_c and DQS_t signals. If the value on DQ0 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired devices and mode registers using MRS command and DQ0.
6. In the 'per DRAM addressability' mode, only MRS commands are allowed.
7. The mode register set command cycle time at PDA mode, AL + CWL + 3.5nCK + tMRD_PDA is required to complete the write operation to the mode register and is the minimum time required between two MRS commands.
8. Remove the DRAM from 'per DRAM addressability' mode by setting MR3 bit "A4=0". (This command will require DQ0=0 for x4, 8, x16).

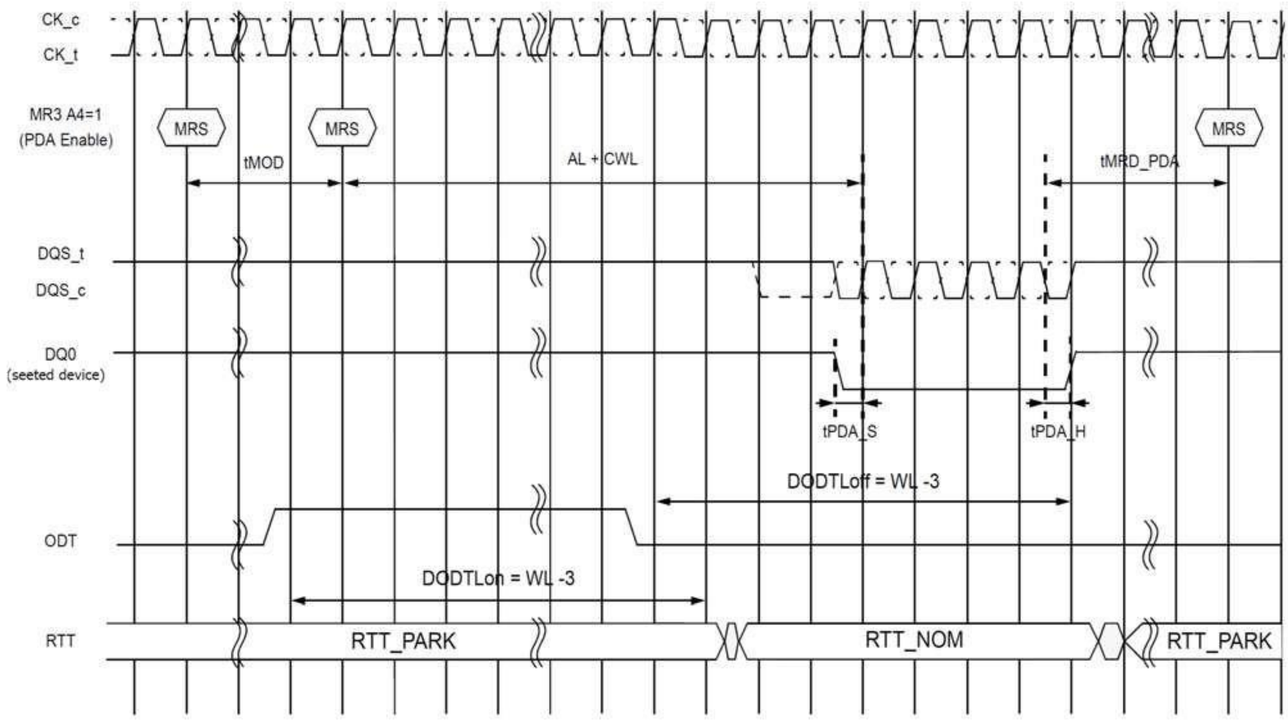
Note: Removing a DRAM from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per DRAM values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case, the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls.

In per DRAM addressability mode, DRAM captures DQ0 using DQS_t and DQS_c like normal write operation. However, Dynamic ODT is not supported. Extra care is required for the ODT setting. If RTT_NOM MR1 [10:8] = Enable, DDR4 SDRAM data termination need to be controlled by ODT pin and apply the same timing parameters as defined in Direct ODT function.

Applied ODT Timing Parameter to PDA Mode

Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay

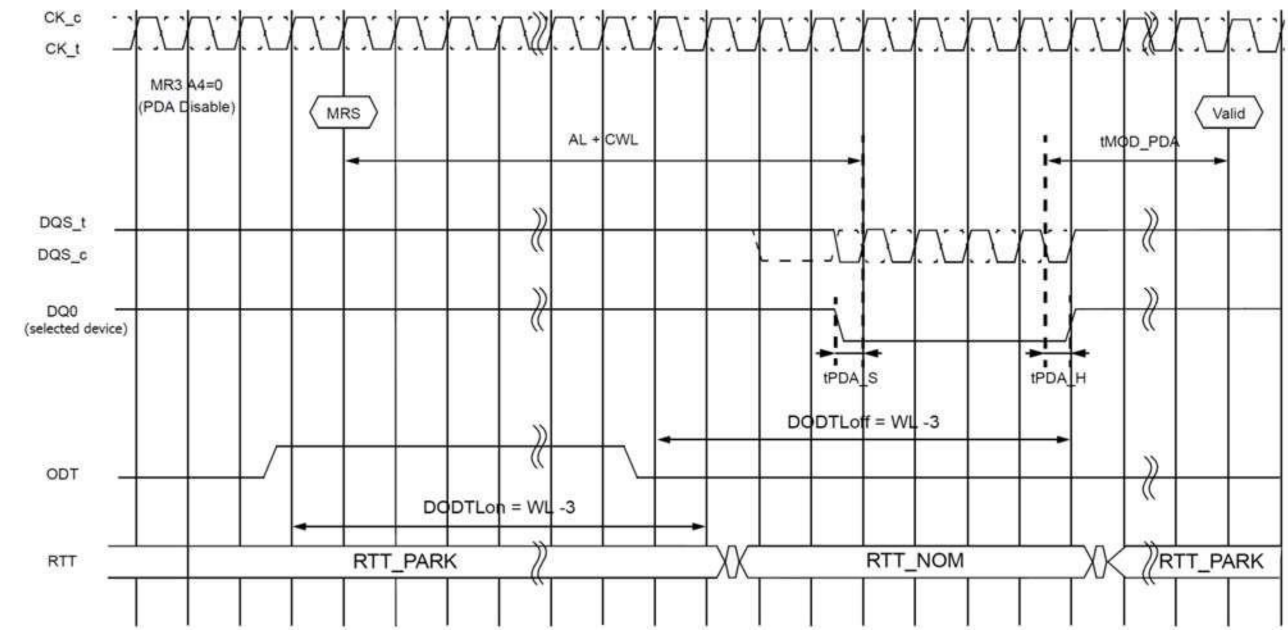
MRS w/ per DRAM addressability (PDA) issuing before MRS



NOTE

RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON

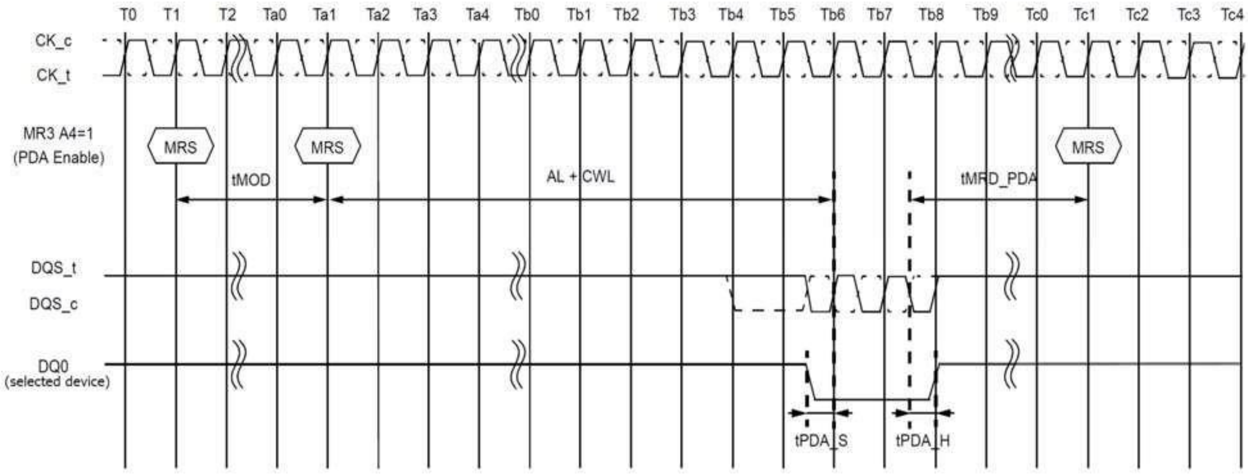
MRS w/ per DRAM addressability (PDA) Exit



NOTE

RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON

PDA using Burst Chop 4



tPDA_S = tDS and tPDA_H = tDH for all DDR4 speed bins.

Since PDA mode may be used to program optimal VREF for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges.

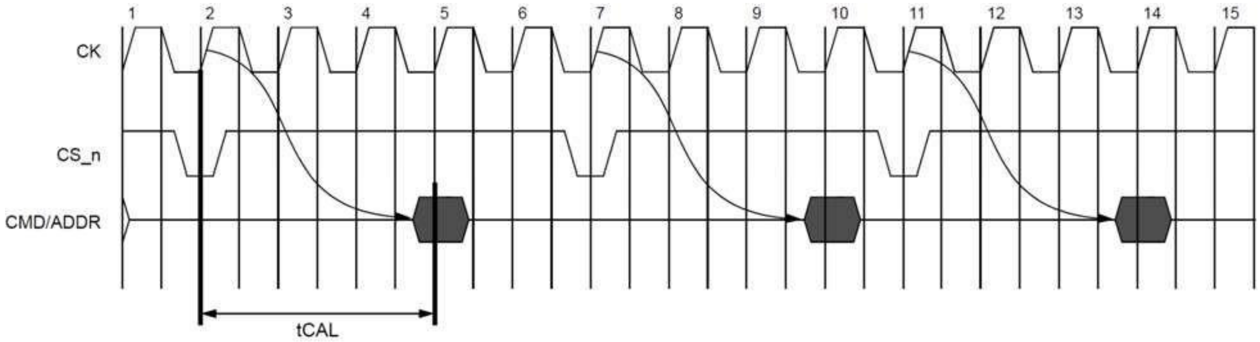
This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 to a 'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

CAL Mode (CS_n to Command Address Latency)

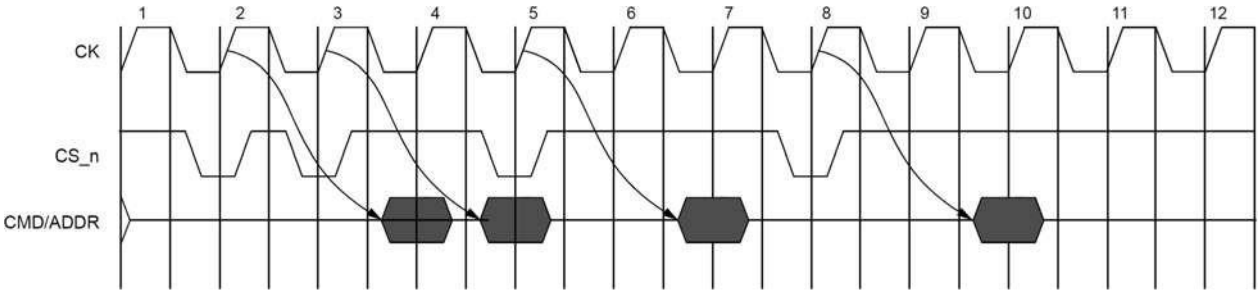
DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between CS_n and CMD/ADDR defined by MR4[A8:A6].

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched,the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence.

Definition of CAL



CAL operational timing for consecutive command issues



The following tables show the timing requirements for tCAL and MRS settings at defferent data rates.

CS to Command Address Latency

Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Unit
CS to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)				nCK

NOTE Geardown mode is not supported for speed bins below DDR4-2666.

Parameter	Symbol	DDR4-2666	DDR4-2933	DDR4-3200	Unit
CS to Command Address Latency	tCAL	max(3 nCK, 3.748 ns)			nCK

NOTE
In geardown mode, odd nCK values for tCAL are not supported, and nCK values must be rounded up to the next higher even integer.

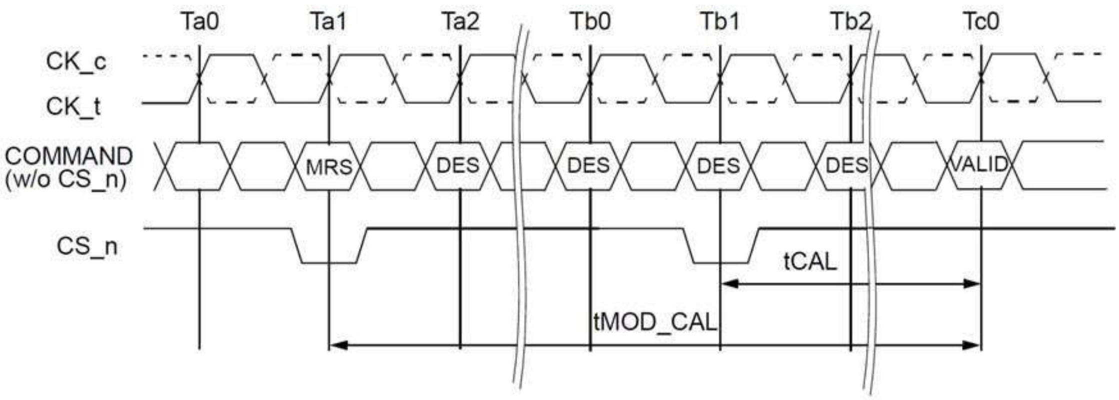
MRS settings for CAL

A8:A6 @ MR4	CAL(tCK cycles)
000	default(disable)
001	3
010	4
011	5
100	6
101	8
110	Reserve
111	Reserve

MRS Timings with Command/Address Latency enabled

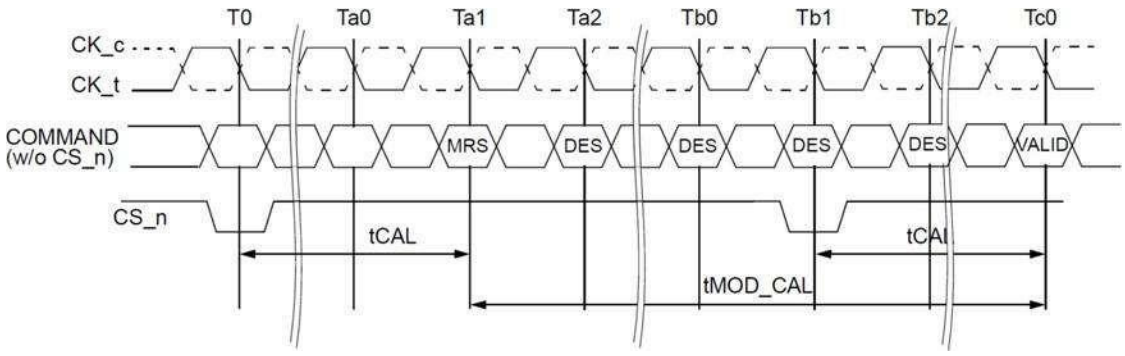
When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, where tMOD_CAL=tMOD+tCAL.

CAL enable timing - tMOD_CAL



NOTE
1. MRS command at Ta1 enables CAL mode
2. tMOD_CAL=tMOD+tCAL

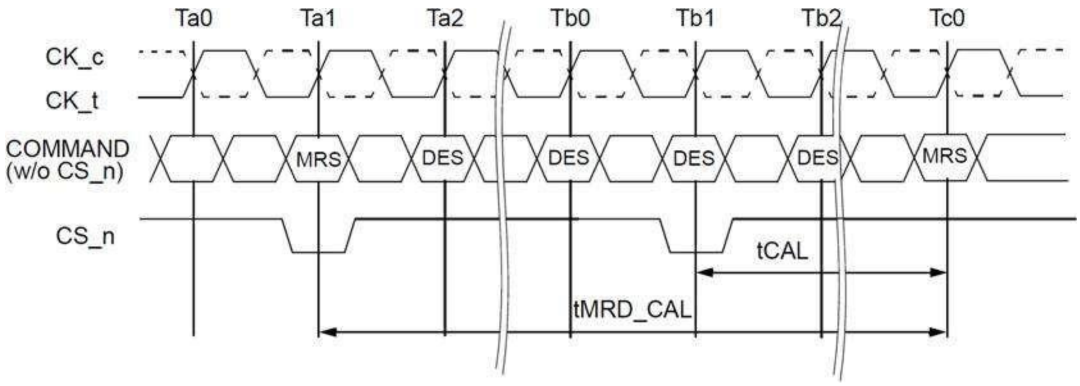
tMOD_CAL, MRS to valid command timing with CAL enabled



NOTE
1. MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting.
2. tMOD_CAL=tMOD+tCAL.

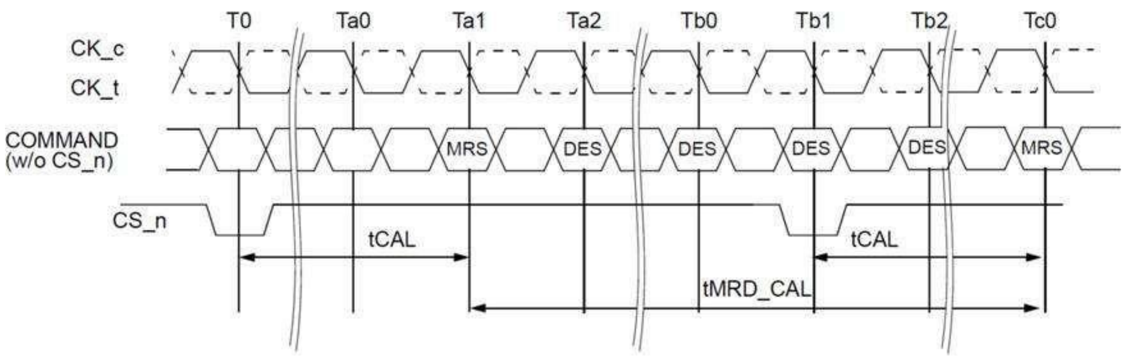
When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_CAL=tMOD+tCAL.

CAL enabling MRS to next MRS command, tMRD_CAL



NOTE
1. MRS command at Ta1 enables CAL mode.
2. tMRD_CAL=tMOD+tCAL.

tMRD_CAL, mode register cycle time with CAL enabled



NOTE
1. MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.
2. tMRD_CAL=tMOD+tCAL.

CRC

CRC Polynomial and logic equation

DDR4 supports CRC for write operation, and doesn't support CRC for read operation.

The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

CRC Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC Combinatorial Logic Equations

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
//initial condition all 0 implied
// "^" = XOR
function [7:0]
nextCRC8_D72;
input [71:0] Data;
input [71:0] D;
reg [7:0] CRC;
begin
D = Data;

  NewCRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
              D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
              D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
              D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
             D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;

  NewCRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
              D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
              D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
              D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
              D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
             D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];

  NewCRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
              D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
              D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
              D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
              D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
```

```
NewCRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
            D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
            D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
            D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
            D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];

NewCRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
            D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
            D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
            D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
            D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];

NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
            D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
            D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
            D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
            D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];

NewCRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
            D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
            D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
            D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
            D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];

NewCRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
            D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
            D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
            D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
            D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;
```

CRC Data Bit Mapping

The Controller generates the CRC checksum and forms the write data frames as below tables.The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the signal if there is a mis-match.DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core, then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

CRC Data Mapping for x4 Devices, BL8

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are ‘1’s.

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	CRC4
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	CRC5
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	CRC6
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	CRC7

CRC Data Mapping for x8 Devices, BL8

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of thelane if DBI function is enabled. A x8 device has a CRC tree with 72 input bits. The 8 bits D[71:64] are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the 8 bits D[71:64] are '1's.

	Transfer Burst Bit									
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
DM_n DBI_n	D64	D65	D66	D67	D68	D69	D70	D71	1	1

CRC Data Mapping for x16 Devices, BL8

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBIL_n and DBIU_n lanes if DBI function is enabled. A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used if either Write DBI or DM is enabled. Note that Write DBI and DM function cannot be enabled simultaneously. If both Write DBI and DM is disabled then the inputs of the upper 8 bits D[143:136] and D[71:64] are '1's.

A x16 device is treated as two x8 devices; a x16 device will have two identical CRC trees implemented. CRC[7:0] covers data bits D[71:0], and CRC[15:8] covers data bits D[143:72].

	Transfer Burst Bit									
	0	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
DQ0	D0	D1	D2	D3	D4	D5	D6	D7	CRC0	1
DQ1	D8	D9	D10	D11	D12	D13	D14	D15	CRC1	1
DQ2	D16	D17	D18	D19	D20	D21	D22	D23	CRC2	1
DQ3	D24	D25	D26	D27	D28	D29	D30	D31	CRC3	1
DQ4	D32	D33	D34	D35	D36	D37	D38	D39	CRC4	1
DQ5	D40	D41	D42	D43	D44	D45	D46	D47	CRC5	1
DQ6	D48	D49	D50	D51	D52	D53	D54	D55	CRC6	1
DQ7	D56	D57	D58	D59	D60	D61	D62	D63	CRC7	1
LDM_n LDBI_n	D64	D65	D66	D67	D68	D69	D70	D71	1	1
DQ8	D72	D73	D74	D75	D76	D77	D78	D79	CRC8	1
DQ9	D80	D81	D82	D83	D84	D85	D86	D87	CRC9	1
DQ10	D88	D89	D90	D91	D92	D93	D94	D95	CRC10	1
DQ11	D96	D97	D98	D99	D100	D101	D102	D103	CRC11	1
DQ12	D104	D105	D106	D107	D108	D109	D110	D111	CRC12	1
DQ13	D112	D113	D114	D115	D116	D117	D118	D119	CRC13	1
DQ14	D120	D121	D122	D123	D124	D125	D126	D127	CRC14	1
DQ15	D128	D129	D130	D131	D132	D133	D134	D135	CRC15	1
UDM_n UDBI_n	D136	D137	D138	D139	D140	D141	D142	D143	1	1

CRC Error Handling

CRC Error mechanism shares the same Alert_n signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

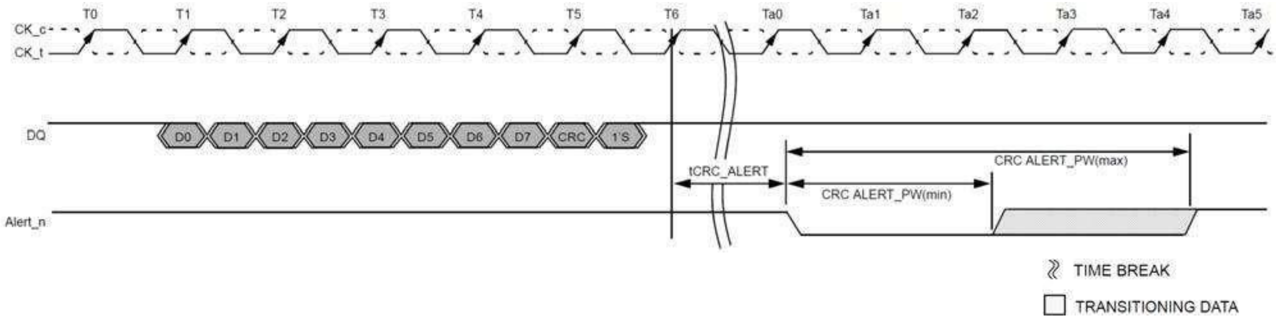
To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is 2 clocks. The latency to Alert_n signal is defined as tCRC_ALERT in the figure below.

DRAM will set CRC Error Clear bit in A4 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for Alert_n (during init) and can backup the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than two clocks at the controller if there are multiple CRC errors as the Alert_n is a daisy chain bus.

CRC Error Reporting



NOTE
1. CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
2. Timing diagram applies to x4, x8, and x16 devices.

CRC Error Timing Parmeters

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
		min	max	min	max	min	max	min	max	
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	-	13	ns
CRC ALERT_n pulse width	CRC ALERT_PW	6	10	6	10	6	10	6	10	nCK

Parameter	Symbol	DDR4-2666		DDR4-2933		DDR4-3200		Unit
		min	max	min	max	min	max	
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	ns
CRC ALERT_n pulse width	CRC ALERT_PW	6	10	6	10	6	10	nCK

CRC Frame Format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

CRC Data Bit Mapping for x4 Devices (BC4)

For a x4 device, the CRC tree inputs are 16 data bits; and the inputs for the remaining bits are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8] and so forth for the CRC tree.

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
A2=0										
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	CRC4
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	CRC5
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	CRC6
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	CRC7
A2=1										
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	CRC4
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	CRC5
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	CRC6
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	CRC7

CRC Data Bit Mapping for x8 Devices (BC4)

For a x8 device, the CRC tree inputs are 36 data bits in transfer's four through seven as 1's.

When A2 = 0, the input bits D[67:64]) are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64]) are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs to D[11:8], and so forth, for the CRC tree. The input bits D[71:68]) are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68]) are 1.

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
A2=0										
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
DM_n DBI_n	D64	D65	D66	D67	1	1	1	1	1	1

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
A2=1										
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
DM_n DBI_n	D68	D69	D70	D71	1	1	1	1	1	1

CRC Data Bit Mapping for x16 Devices (BC4)

There are two identical CRC trees for x16 devices, each have CRC tree inputs of 36 bits.

When A2 = 0, input bits D[67:64] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[67:64] are 1s. The input bits D[139:136] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[139:136] are 1.

When A2 = 1, data bits D[7:4] are used as inputs for D[3:0], D[15:12] are used as inputs for D[11:8], and so forth, for the CRC tree. Input bits D[71:68] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[71:68] are 1s. The input bits D[143:140] are used if DBI_n or DM_n functions are enabled; if DBI_n and DM_n are disabled, then D[143:140] are 1.

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
A2=0										
DQ0	D0	D1	D2	D3	1	1	1	1	CRC0	1
DQ1	D8	D9	D10	D11	1	1	1	1	CRC1	1
DQ2	D16	D17	D18	D19	1	1	1	1	CRC2	1
DQ3	D24	D25	D26	D27	1	1	1	1	CRC3	1
DQ4	D32	D33	D34	D35	1	1	1	1	CRC4	1
DQ5	D40	D41	D42	D43	1	1	1	1	CRC5	1
DQ6	D48	D49	D50	D51	1	1	1	1	CRC6	1
DQ7	D56	D57	D58	D59	1	1	1	1	CRC7	1
LDM_n LDBI_n	D64	D65	D66	D67	1	1	1	1	1	1
DQ8	D72	D73	D74	D75	1	1	1	1	CRC8	1
DQ9	D80	D81	D82	D83	1	1	1	1	CRC9	1
DQ10	D88	D89	D90	D91	1	1	1	1	CRC10	1
DQ11	D96	D97	D98	D99	1	1	1	1	CRC11	1
DQ12	D104	D105	D106	D107	1	1	1	1	CRC12	1
DQ13	D112	D113	D114	D115	1	1	1	1	CRC13	1
DQ14	D120	D121	D122	D123	1	1	1	1	CRC14	1
DQ15	D128	D129	D130	D131	1	1	1	1	CRC15	1
UDM_n UDBI_n	D136	D137	D138	D139	1	1	1	1	1	1

	Transfer Burst Bit									
	0	1	2	3	4	5	6	7	8	9
A2=1										
DQ0	D4	D5	D6	D7	1	1	1	1	CRC0	1
DQ1	D12	D13	D14	D15	1	1	1	1	CRC1	1
DQ2	D20	D21	D22	D23	1	1	1	1	CRC2	1
DQ3	D28	D29	D30	D31	1	1	1	1	CRC3	1
DQ4	D36	D37	D38	D39	1	1	1	1	CRC4	1
DQ5	D44	D45	D46	D47	1	1	1	1	CRC5	1
DQ6	D52	D53	D54	D55	1	1	1	1	CRC6	1
DQ7	D60	D61	D62	D63	1	1	1	1	CRC7	1
LDM_n LDBI_n	D68	D69	D70	D71	1	1	1	1	1	1
DQ8	D76	D77	D78	D79	1	1	1	1	CRC8	1
DQ9	D84	D85	D86	D87	1	1	1	1	CRC9	1
DQ10	D92	D93	D94	D95	1	1	1	1	CRC10	1
DQ11	D100	D101	D102	D103	1	1	1	1	CRC11	1
DQ12	D108	D109	D110	D111	1	1	1	1	CRC12	1
DQ13	D116	D117	D118	D119	1	1	1	1	CRC13	1
DQ14	D124	D125	D126	D127	1	1	1	1	CRC14	1
DQ15	D132	D133	D134	D135	1	1	1	1	CRC15	1
UDM_n UDBI_n	D140	D141	D142	D143	1	1	1	1	1	1

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19] ^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;

CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1 ^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];

CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^ D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];

CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^ D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];

CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^ D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];

CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^ D[47]=1 ^ D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18] ^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;

CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;

CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1 ^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];

CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29] ^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];

CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1 ^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];

CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];

CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1 ^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];

CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[37] ^ D[36] ^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data.

CRC Simultaneous Operation Restrictions

When write CRC is enabled, neither MPR writes nor per-DRAM mode is allowed.

Command Address Parity (CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register when C/A Parity is enabled (Parity Latency) and is applied to all commands.When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus including bank address and bank group bits. The control signals CKE, ODT and CS_n are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0’s, e.g., if a common die has stacked pins but the device is used in a monolithic application then the address pins used for stacking should internally be treated as 0’s)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1’s in the transmitted signal, including the parity bit, is even.

If a DRAM detects a C/A parity error in any command as qualified by CS_n then it must perform the following steps:

- Ignore the erroneous command. Commands in max NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the DRAM does not activate DQS outputs.
- Log the error by storing the erroneous command and address bits in the error log. (MPR page1)
- Set the Parity Error Status bit in the mode register to ‘1’. The Parity Error Status bit must be set before the ALERT_n signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).
- Assert the ALERT_n signal to the host (ALERT_n is active low) within tPAR_ALERT_ON time.
- Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command. If a parity error occurs on a command issued between the tXS_Fast and tXS window after self-refresh exit then the DRAM may delay the de-assertion of ALERT_n signal as a result of any internal on going refresh.
- Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR_ALERT_ON + tPAR_ALERT_PW).
- After tPAR_ALERT_PW_min has been satisfied, the DRAM may de-assert ALERT_n.
- After the DRAM has returned to a known pre-charged state it may de-assert ALERT_n.
- After (tPAR_ALERT_ON + tPAR_ALERT_PW), the DRAM is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a ‘0’(the DRAM will execute any erroneous commands until the bit is cleared).
- It is possible that the DRAM might have ignored a refresh command during the (tPAR_ALERT_ON + tPAR_ALERT_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.
- The Parity Error Status bit may be read anytime after (tPAR_ALERT_ON + tPAR_ALERT_PW) to determine which DRAM had the error. The DRAM maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to ‘0’.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The controller can only program the Parity Error Status bit to ‘0’. If the controller illegally attempts to write a ‘1’ to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a ‘1’ to the Parity Error Status bit.

DDR4 SDRAM supports MR bit for ‘Persistent Parity Error Mode’. This mode is enabled by setting MR5 A9=High and when it is enabled, DRAM resumes checking CA Parity after the alert_n is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the Error log in MPR page 1 should be treated as ‘Don’t Care’. In ‘Persistent Parity Error Mode’ the Alert_n pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR_ALERT_PW. The controller must issue DESELECT com-mands once it detects the Alert_n signal, this response time is defined as tPAR_ALERT_RSP.

Mode Register Setting for CA Parity

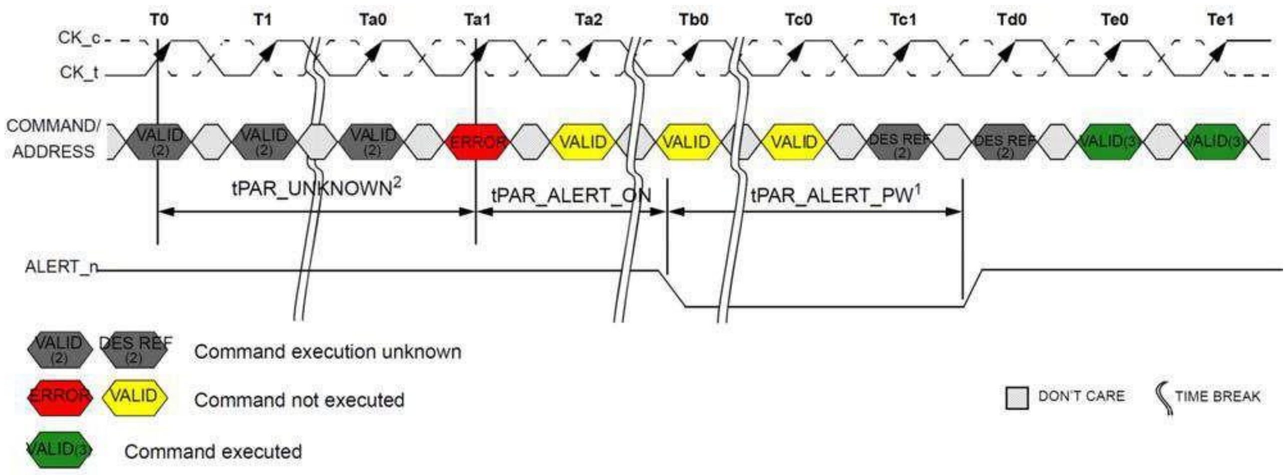
C/A Parity Latency MR5[2:0][1]	Speed bins	C/A Parity Error Status MR5[4]	Parity Persistent Mode MR5[9]	Errant C/A Frame
000 = Disabled	-	0=clear	0 = Disabled	C2-C0, ACT_n, BG1, BG0, BA0, BA1, PAR, A17, A16/RAS_n, A15/CAS_n, A14/WE_n, A13:A0
001= 4 Clocks	1600,1866,2133			
010= 5 Clocks	2400	1=Error	1 = Enabled	
011= 6 Clocks	RFU			
100= 8 Clocks	RFU			

NOTE

1. Parity Latency is applied to all commands.
2. Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL=3 PL=4 is not allowed. Correct sequence is PL=3 → Disabled → PL=4
3. Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

The following figure captures the flow of events on the C/A bus and the ALERT_n signal.

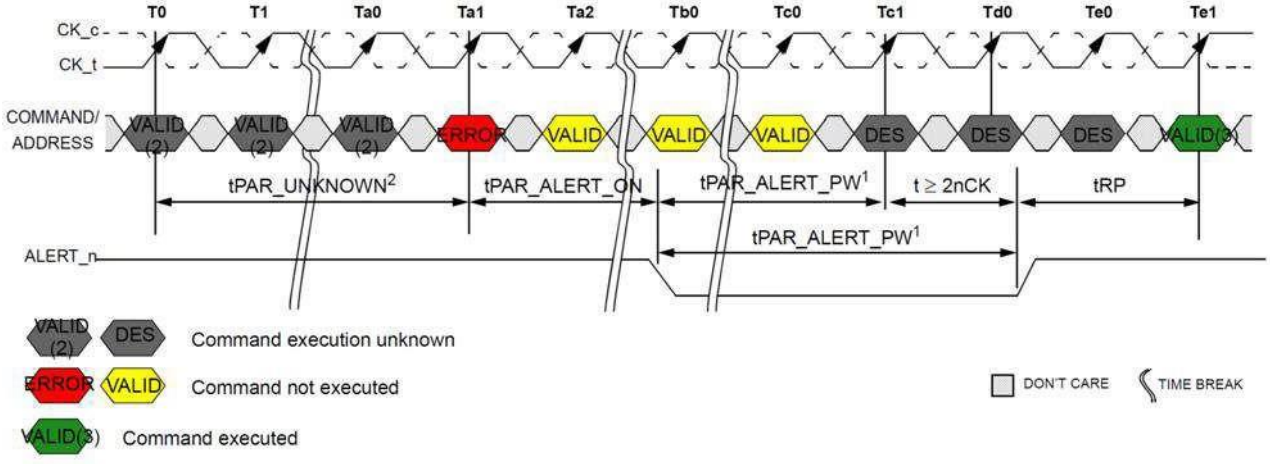
Normal CA Parity Error Checking Operation



NOTE

1. DRAM is emptying queues. Precharge all and parity checking off until Parity Error Statusbit cleared.
2. Command execution is unknown; the corresponding DRAM internal state change mayor may not occur. The DRAM controller should consider both cases and make sure thatthe command sequence meets the specifications.
3. Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Paritychecking off until Parity Error Status bit cleared.

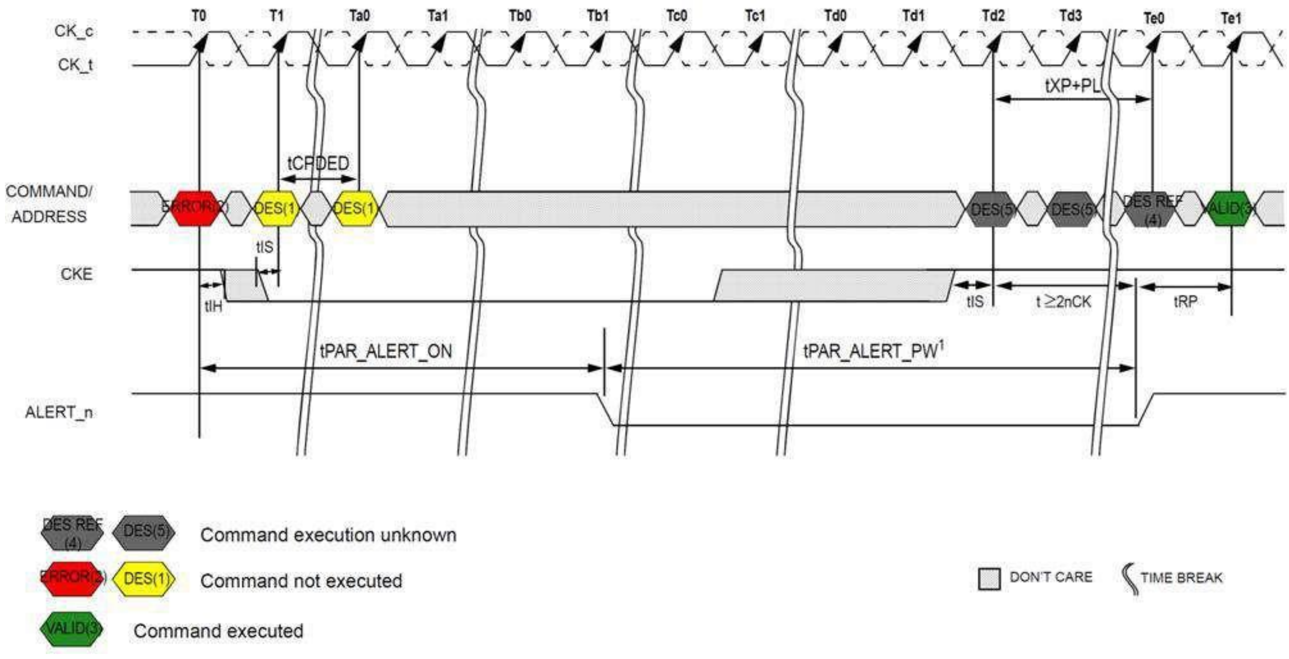
Persistent CA Parity Error Checking Operation



NOTE

1. DRAM is emptying queues. Precharge all and parity check re-enable finished bytPAR_ALERT_PW.
2. Command execution is unknown; the corresponding DRAM internal state change mayor may not occur. The DRAM controller should consider both cases and make sure thatthe command sequence meets the specifications.
3. Normal operation with parity latency and parity checking (CA Parity Persistent ErrorMode enabled).

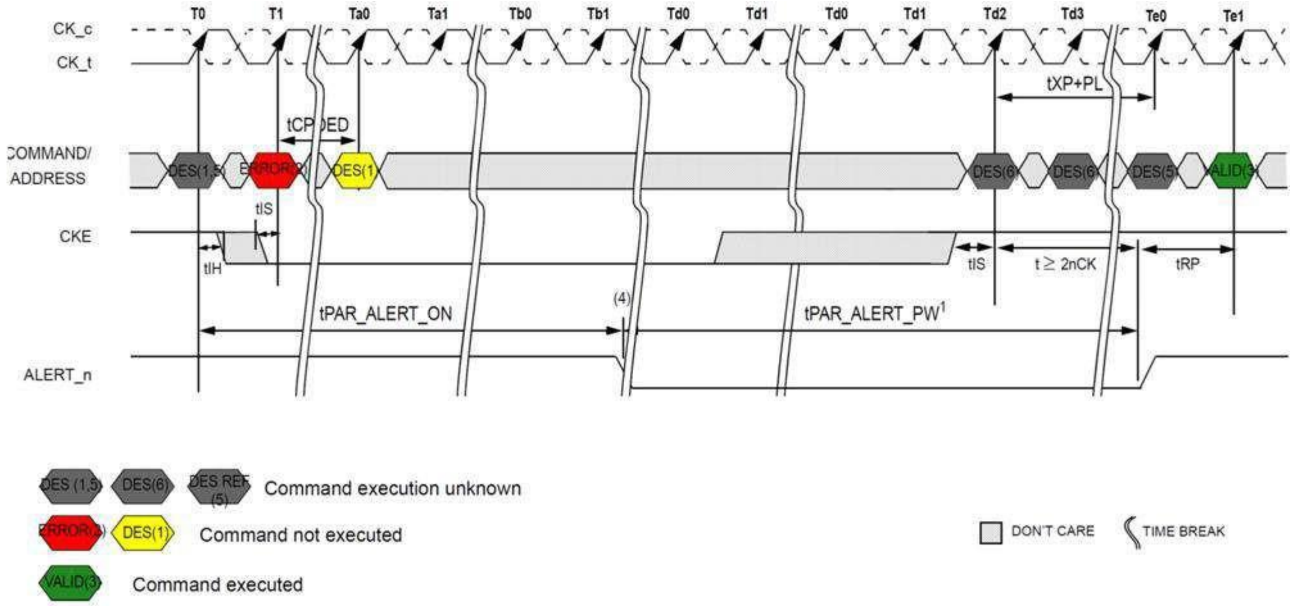
CA Parity Error Checking - PDE/PDX



NOTE

1. Deselect command only allowed.
2. Error could be Precharge or Activate.
3. Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Paritychecking is off until Parity Error Status bit cleared.
4. Command execution is unknown; the corresponding DRAM internal state change mayor may not occur. The DRAM controller should consider both cases and make sure thatthe command sequence meets the specifications.
5. Deselect command only allowed; CKE may go high prior to Td2 as long as DES commandsare issued.

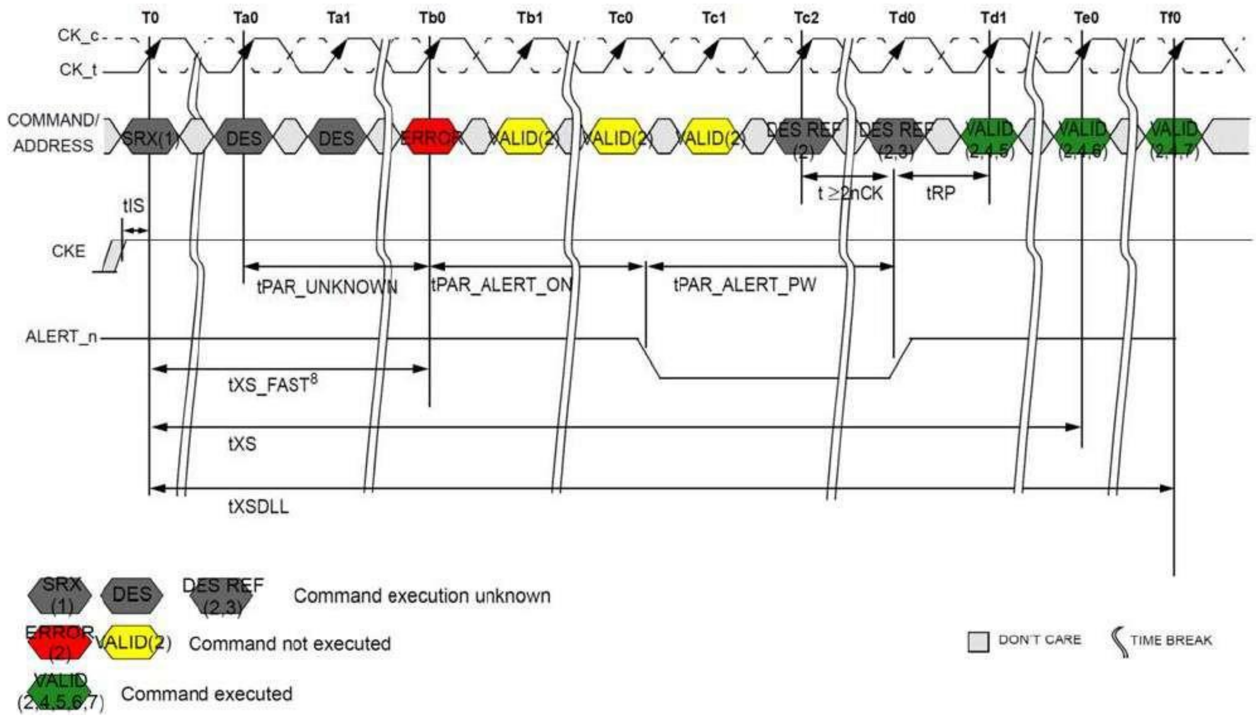
CA Parity Error Checking - SRE Attempt



NOTE

1. Deselect command only allowed.
2. Self Refresh command error. DRAM masks the intended SRE command and enters PrechargePower Down.
3. Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Paritychecking is off until Parity Error Status bit cleared.
4. Controller cannot disable clock until it has been able to have detected a possible C/AParity error.
5. Command execution is unknown; the corresponding DRAM internal state change mayor may not occur. The DRAM controller should consider both cases and make sure thatthe command sequence meets the specifications.
6. Deselect command only allowed; CKE may go high prior to Tc2 as long as DES commandsare issued.

CA Parity Error Checking – SRX



NOTE
1. Self Refresh Abort = Disable: MR4 A[9] = 0.
2. Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.
3. Command execution is unknown; the corresponding DRAM internal state change mayor may not occur. The DRAM controller should consider both cases and make sure thatthe command sequence meets the specifications.
4. Normal operation with parity latency (CA Parity Persistent Error Mode disabled). Paritychecking off until Parity Error Status bit cleared.
5. Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS, orZQCL command allowed
6. Valid commands not requiring a locked DLL.
7. Valid commands requiring a locked DLL.
8. This figure shows the case from which the error occurred after tXS_FAST. An error mayalso occur after tXS_ABORT and tXS.

Command/Address parity entry and exit timings

When in CA Parity mode, including entering and exiting CA Parity mode, users must wait tMRD_PAR before issuing another MRS command, and wait tMOD_PAR before any other commands.

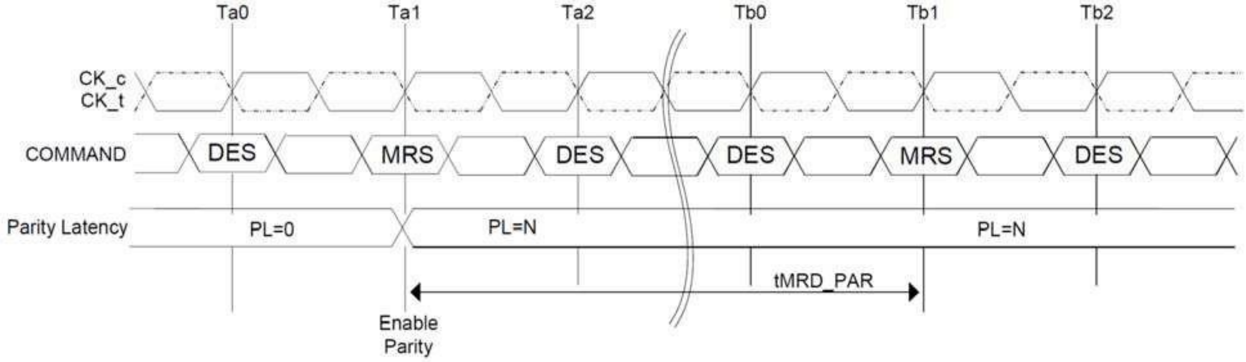
tMOD_PAR = tMOD + PL

tMRD_PAR = tMOD + PL

For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.

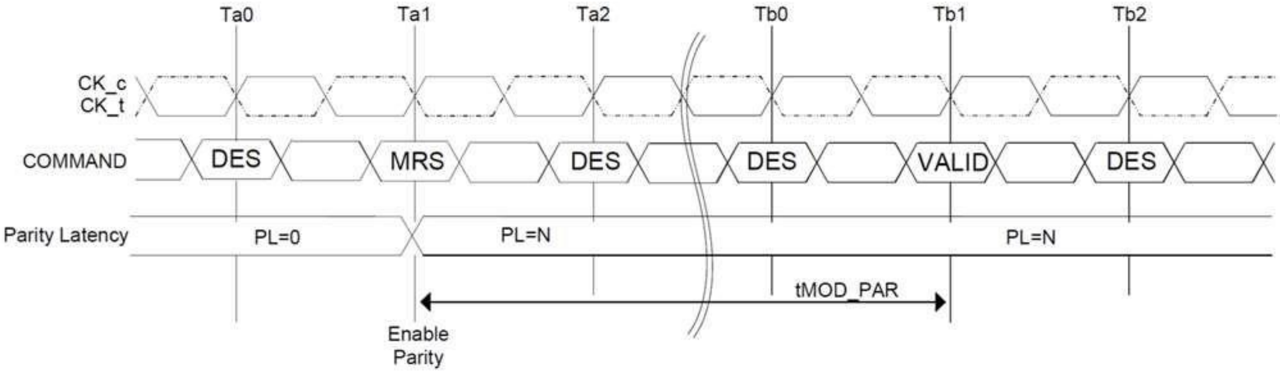
For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.

Parity entry timing example - tMRD_PAR



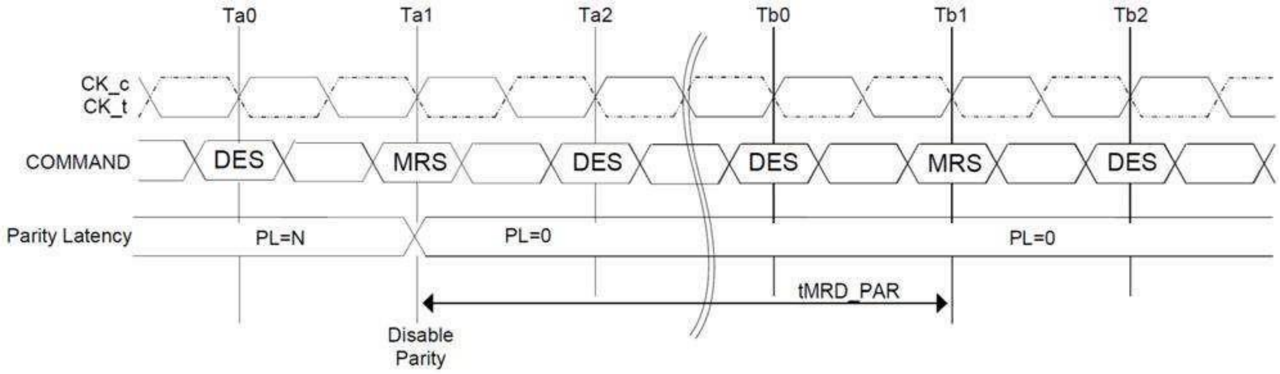
NOTE tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity entry timing example - tMOD_PAR



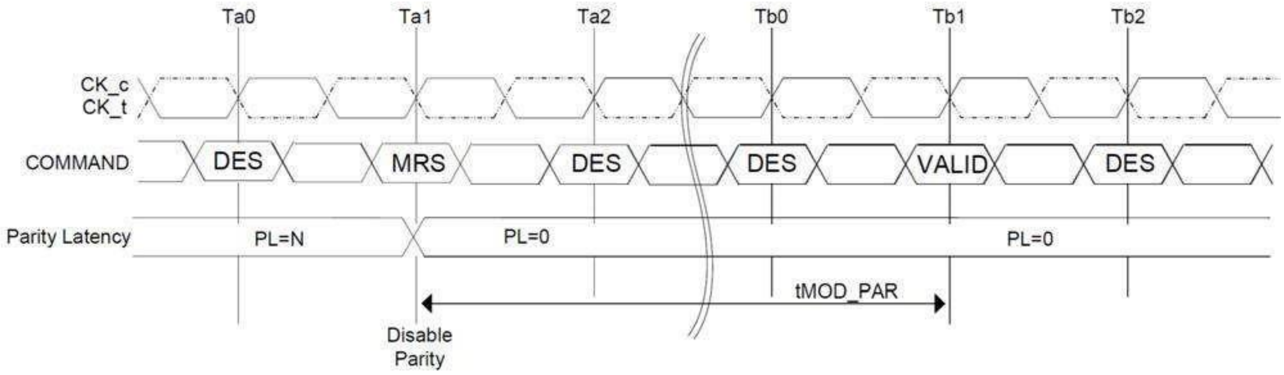
NOTE tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Parity exit timing example - tMRD_PAR



NOTE tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Parity exit timing example - tMOD_PAR



NOTE tMOD_PAR = tMOD + N; where N is the programmed parity latency.

CA Parity Error Log Readout

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BA1:BA0 = 0:1	00=MPR0	A7	A6	A5	A4	A3	A2	A1	A0
	01=MPR1	CAS_n/ A15	WE_n/A14	A13	A12	A11	A10	A9	A8
	10=MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/ A16
	11=MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency			C2	C1	C0

NOTE

1. MPR used for CA parity error log readout is enabled by setting A[2] in MR3
2. For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
3. If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

Gear Down Mode

The following sequence represents for the gear down mode. The DRAM defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE and ODT in 1/4 rate(2N) mode. For operation in 1/2 rate mode, no MRS command for geardown or sync pulse is required. DRAM defaults is in 1/2 rate mode.

General sequence for operation in geardown during initialization

1. DRAM defaults to a 1/2 rate(1N mode) internal clock at power up/reset
2. Assertion of reset
3. Assertion of CKE enables the DRAM
4. MRS is accessed with a low frequency N*tck MRS geardown CMD Ntck static MRS command qualified by 1N CS_n
5. DRAM controller sends a 1N sync pulse with a low frequency N*tCK NOP CMD; tSYNC_GEAR is an even number of clocks; sync pulse on even clock boundary from MRS CMD.
6. Initialization sequence, including the expiration of tDLLK and tZQinit, starts in 2N mode after tCMD_GEAR from 1N Sync Pulse.

Initialization sequence, including the expiration of tDLLK and tZQinit, starts in 2N mode after tCMD_GEAR from 1N Sync Pulse.

1. MRS is set to 1, via MR3[3], with a low-frequency N × tCK gear-down MRS command.

    a. The NtCK static MRS command is qualified by 1N CS_n, which meets tXS or tXS_ABORT.

    b. Only a REFRESH command may be issued to the DRAM before the NtCK static MRS command.

2. The DRAM controller sends a 1N sync pulse with a low-frequency N × tCK NOP command.

    a. tSYNC_GEAR is an even number of clocks.

    b. The sync pulse is on even edge clock boundary from the MRS command.

3. A valid command not requiring locked DLL is available in 2N mode after tCMD_GEAR from the 1N sync pulse.

    a. A valid command requiring locked DLL is available in 2N mode after tXSDLL or tDLLK from the 1N sync pulse.

4. If operation is in 1N mode after self refresh exit, N × tCK MRS command or sync pulse is not required during self refresh exit. The minimum exit delay to the first valid command is tXS, or tXS_ABORT.

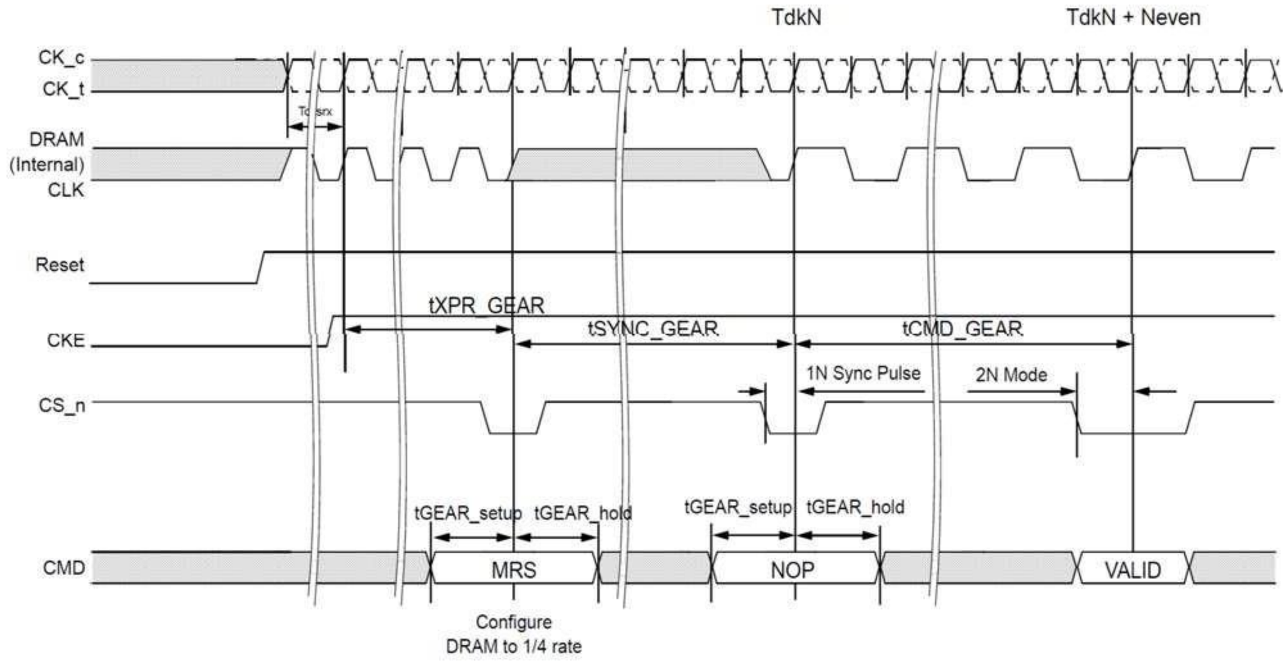
The DRAM may be changed from 1/4(2N) rate to 1/2(1N) rate by entering self refresh mode, which will reset to 1N mode. Changing from 1/4(2N) to 1/2(1N) by any other means can result in loss of data and make operation of the DRAM uncertain.

When operating in 2N gear-down mode, the following MR settings apply:

- CAS latency (MR0[6:4,2]): Even number of clocks
- Write recovery and read to precharge (MR0[11:9]): Even number of clocks
- Additive latency (MR1[4:3]): CL - 2
- CAS WRITE latency (MR2 A[5:3]): Even number of clocks
- CS to command/address latency mode (MR4[8:6]): Even number of clocks
- CA parity latency mode (MR5[2:0]): Even number of clocks

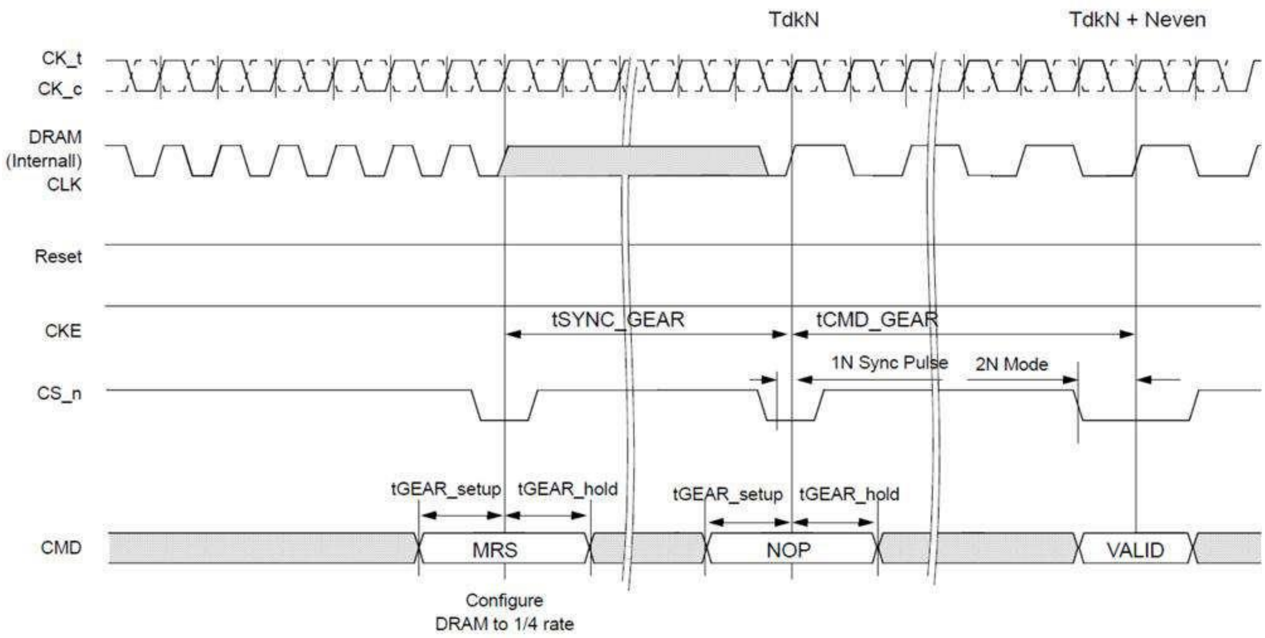
The diagram below illustrates the sequence for control operation in 2N mode during power up.

Gear down (2N) mode entry sequence during initialization

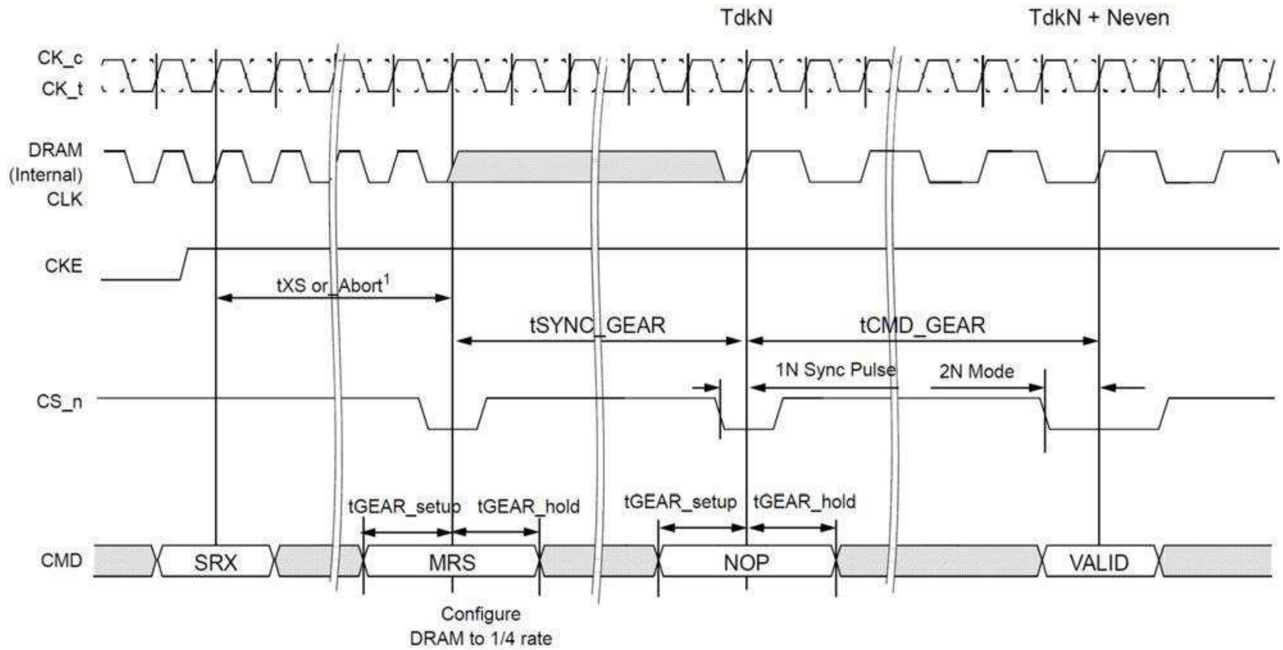


The diagram below represents the operation of geardown (1/2 rate to 1/4 rate) mode during normal operation with CKE and Reset set high.

Gear down (2N) mode entry sequence during normal operation



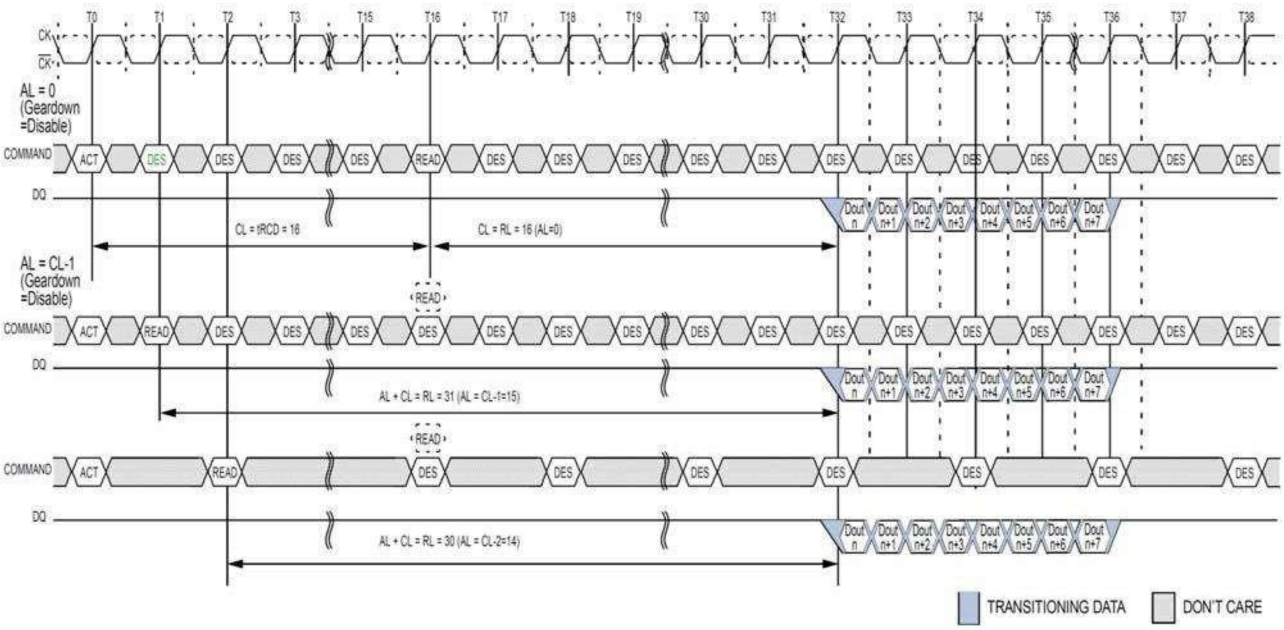
Gear down (2N) mode entry sequence after self refresh exit (SRX)



NOTE CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting is as follows.

- MR4[A9] = 0 : tXS
- MR4[A9] = 1 : tXS_Abort

Comparison Timing Diagram Between Geardown Disable and Enable



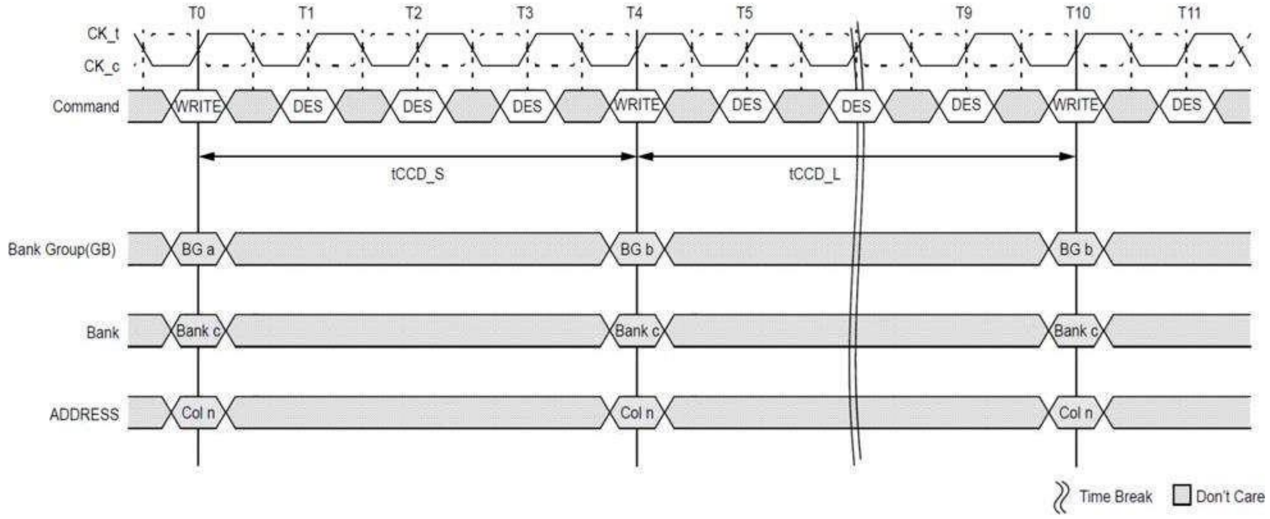
NOTE

1. BL=8, tRCD=CL=16
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Bank Access Operation

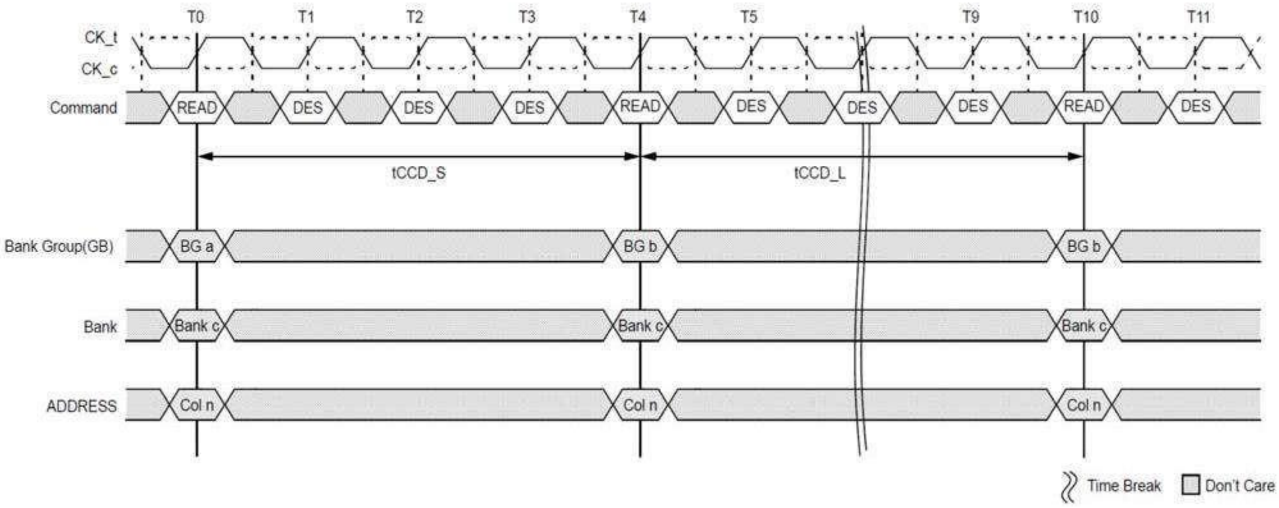
DDR4 supports bank grouping: x4/x8 DRAMs have four Bank Groups (BG[1:0]) and each bank group is comprised of four sub-banks (BA[1:0]); x16 DRAMs have two Bank Groups (BG[0]) and each bank group is comprised of made up of four sub-banks. Bank accesses to different banks groups require less time delay between accesses than Bank accesses to within the same banks group. Bank accesses to different bank groups require tCCD_S short delay between commands while Bank accesses within the same bank group require tCCD_L long delay between commands.

tCCD Timing (WRITE to WRITE Example)



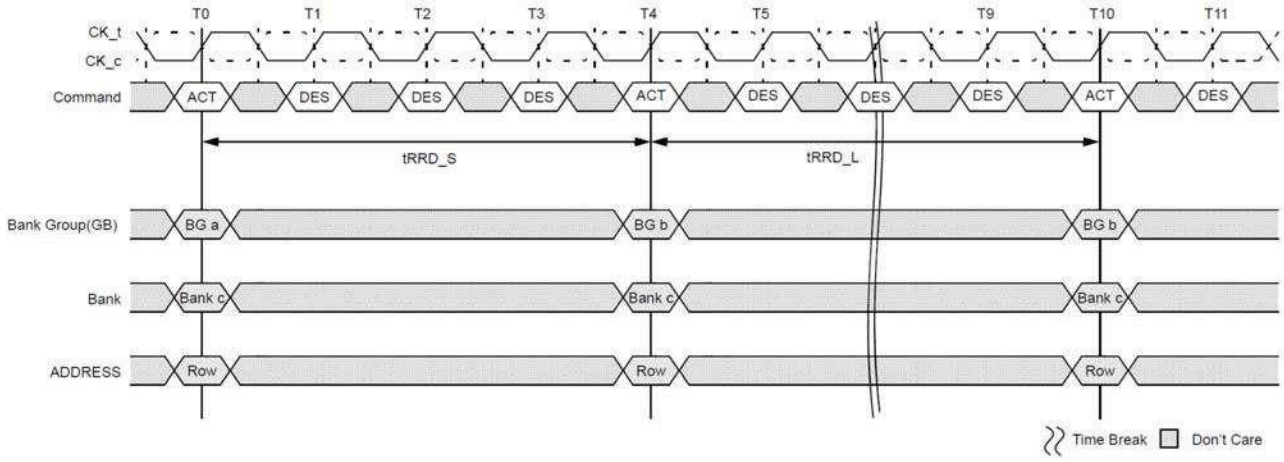
NOTE
1. tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
2. tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

tCCD Timing (READ to READ Example)



NOTE
1. tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
2. tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

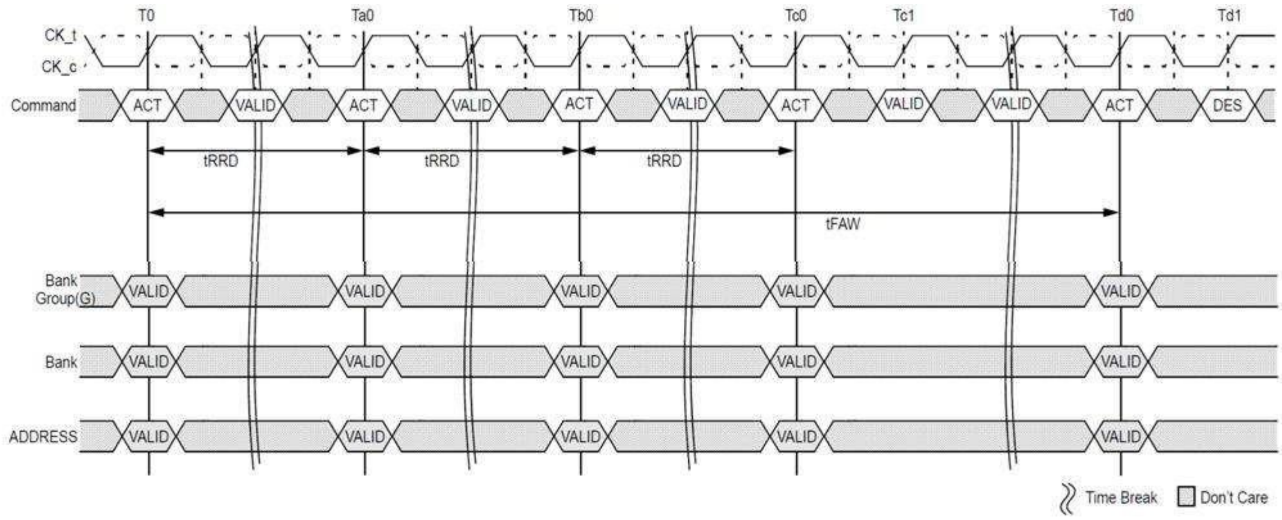
tRRD Timing



NOTE

1. tRRD_S : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e. T0 to T4)
2. tRRD_L : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group (i.e. T4 to T10)

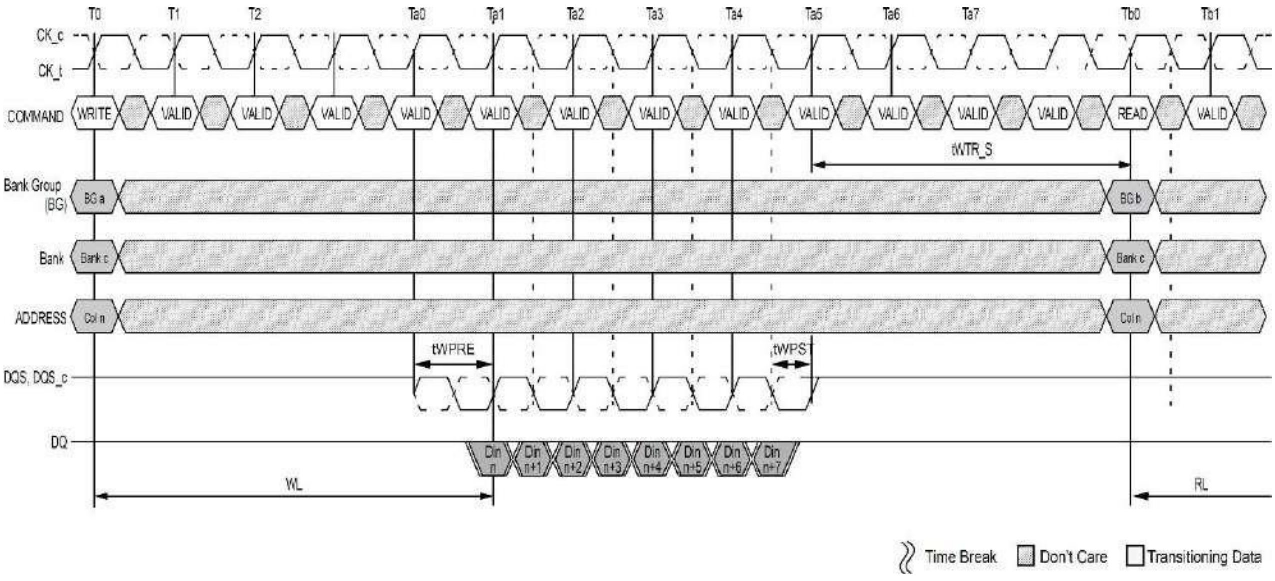
tFAW Timing



NOTE

tFAW : Four activate window

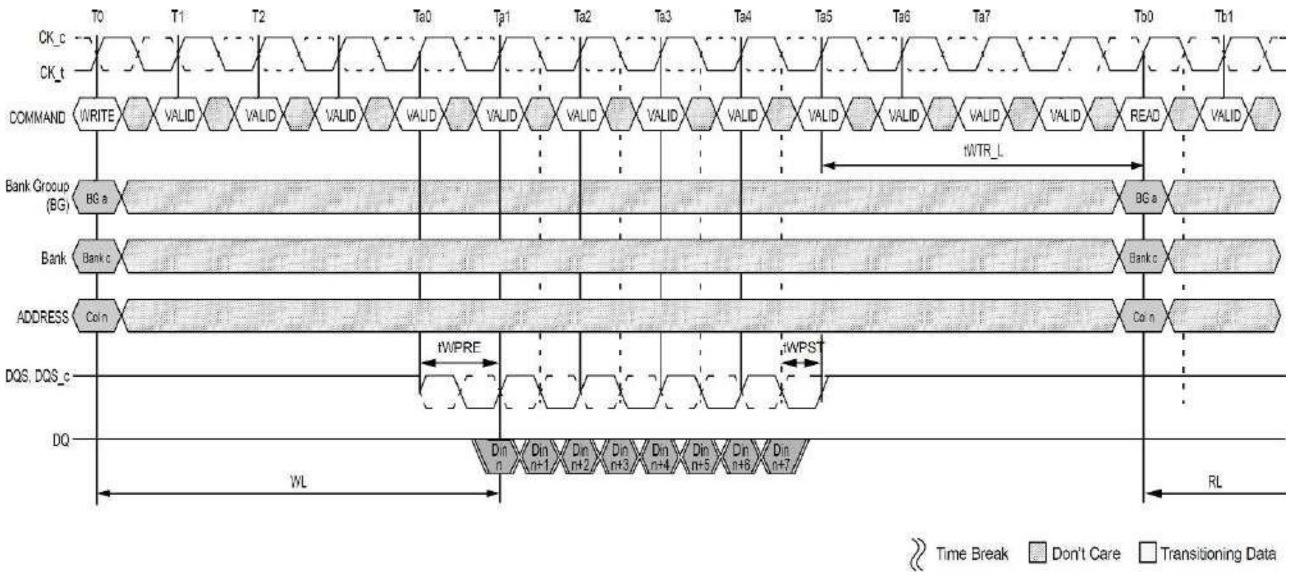
tWTR_S Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)



NOTE

tWTR_S : Delay from start of internal write transaction to internal read command to a different Bank Group

tWTR_L Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)



NOTE

tWTR_L : Delay from start of internal write transaction to internal read command to the same Bank Group

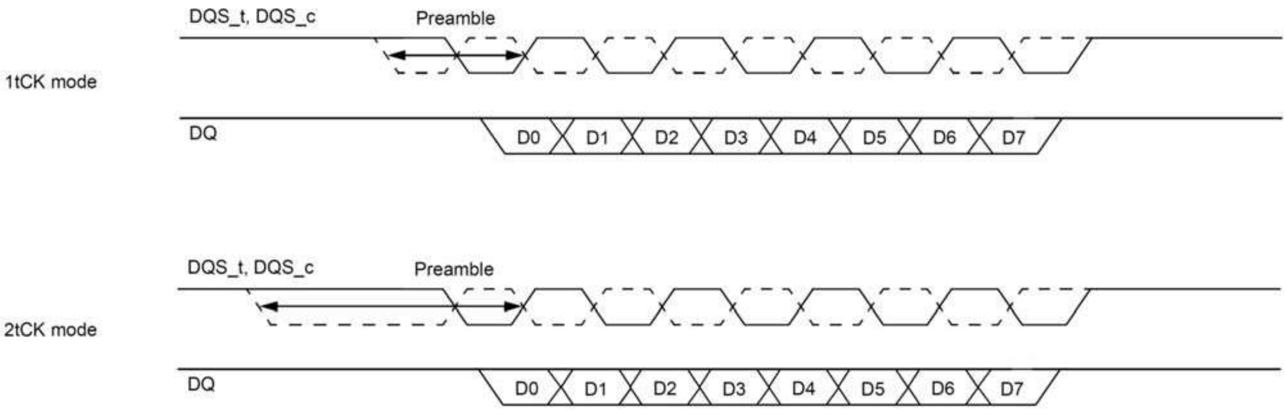
Programmable Preamble

Write Preamble

DDR4 supports a programmable write preamble. Write preamble modes of 1 tCK and 2 tCK are selectable by MR4 [A12].

CWL needs to be incremented by 1nCK when 2tCK preamble is enabled.

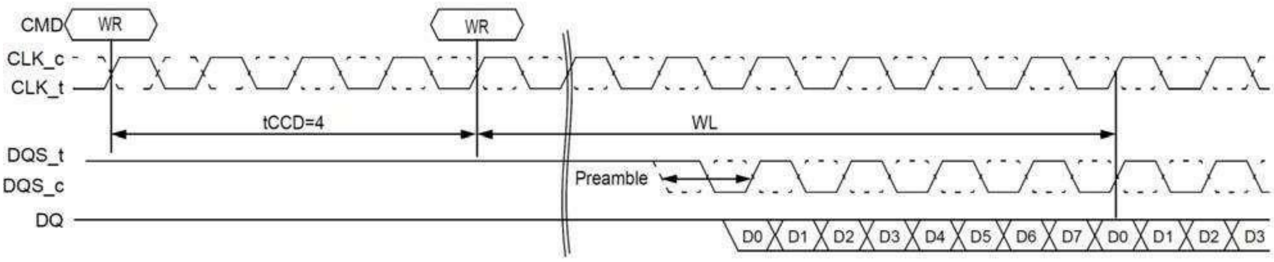
When operating in 2tCK Write Preamble Mode, tWTR and tWR must be programmed to a value 1 clock greater than the tWTR and tWR setting supported in the applicable speed bin.



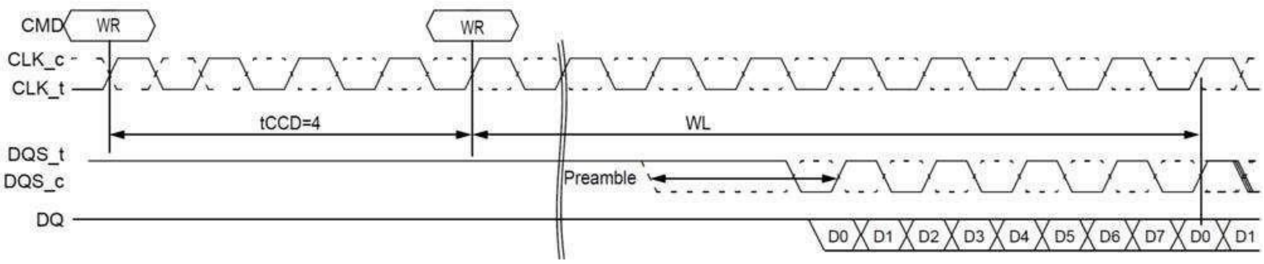
The timing diagrams below illustrate 1 and 2 tCK preamble scenarios for consecutive write commands with tCCD timing of 4, 5 and 6 nCK, respectively. Setting tCCD to 5nCK is not allowed in 2 tCK preamble mode.

tCCD=4 (AL=PL=0)

1tCK mode

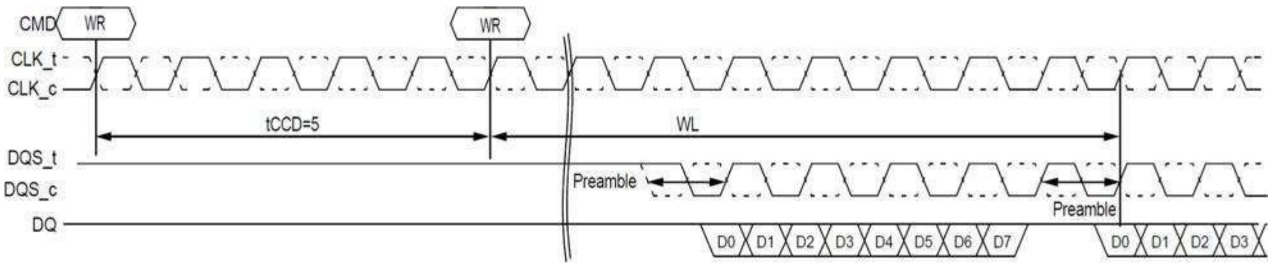


2tCK mode



tCCD=5 (AL=PL=0)

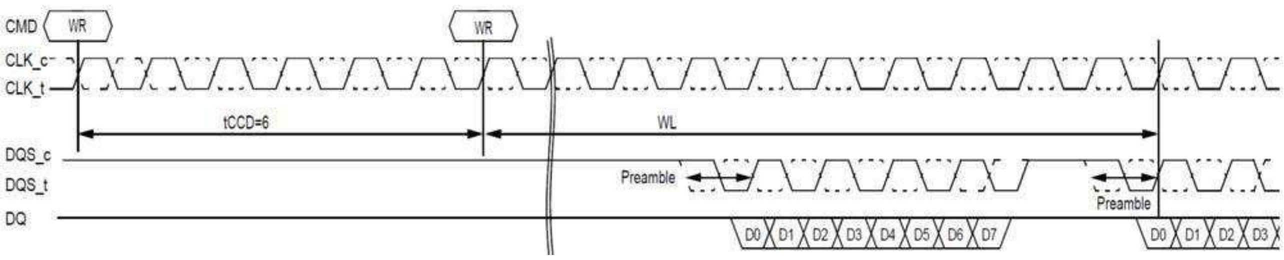
1tCK mode



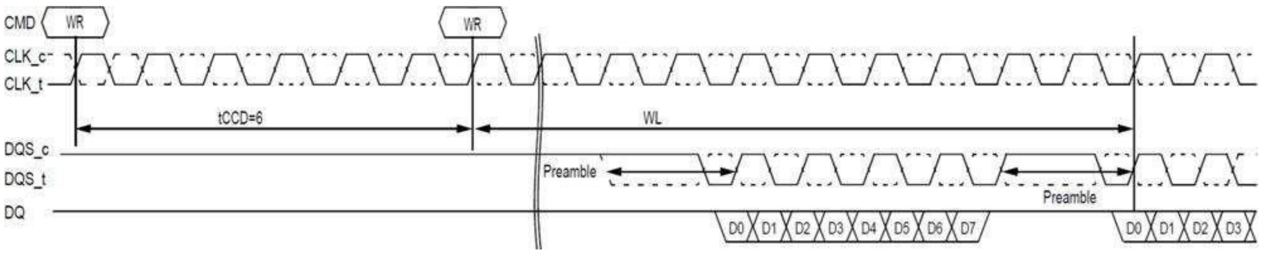
2tCK mode : tCCD=5 is not allowed in 2tCK mode

tCCD=6 (AL=PL=0)

1tCK mode



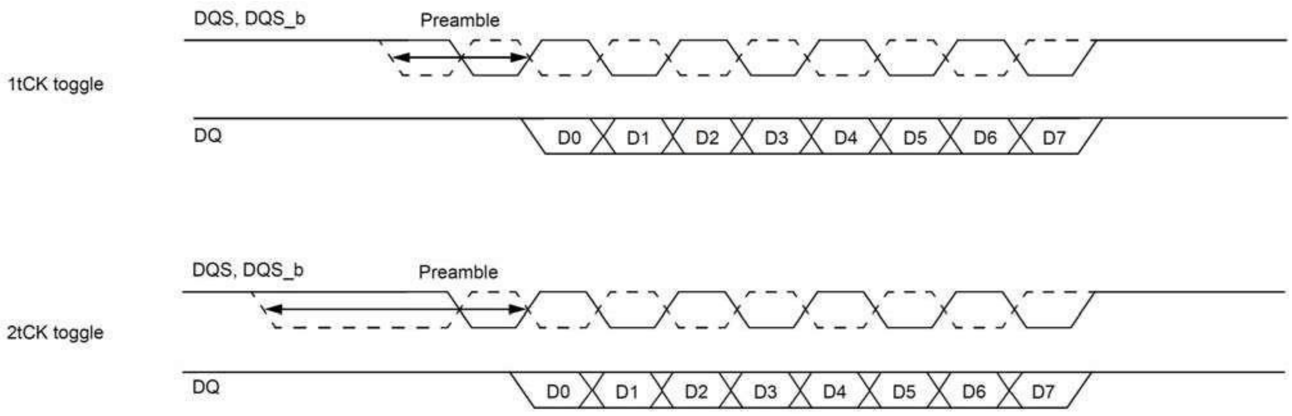
2tCK mode



Read Preamble

DDR4 supports a programmable read preamble. Read preamble modes of 1 tCK and 2 tCK are selectable by MR4 [A11].

Read preamble modes of 1 tCK and 2 tCK are shown below.

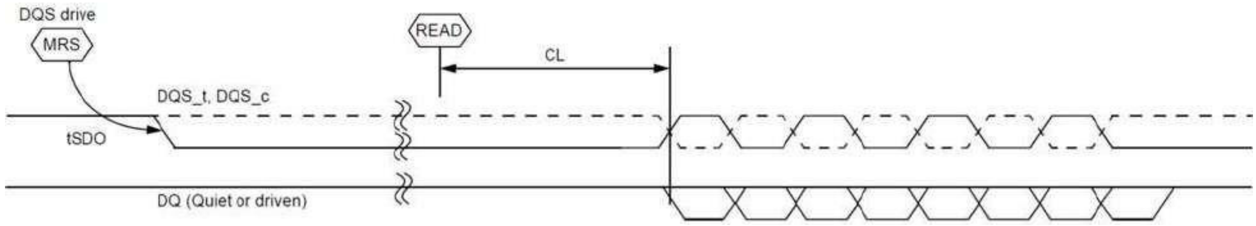


Read Preamble Training

DDR4 supports READ preamble training via MPR reads; that is, READ preamble training is allowed only when the DRAM is in the MPR access mode. The READ preamble training mode can be used by the DRAM controller to train or "read level" its DQS receivers.

READ preamble training is entered via an MRS command (MR4[A10] = 1 is enabled and MR4[A10] = 0 is disabled). After the MRS command is issued to enable READ preamble training, the DRAM DQS signals are driven to a valid level by the time tSDO is satisfied. During this time, the data bus DQ signals are held quiet, that is, driven HIGH.

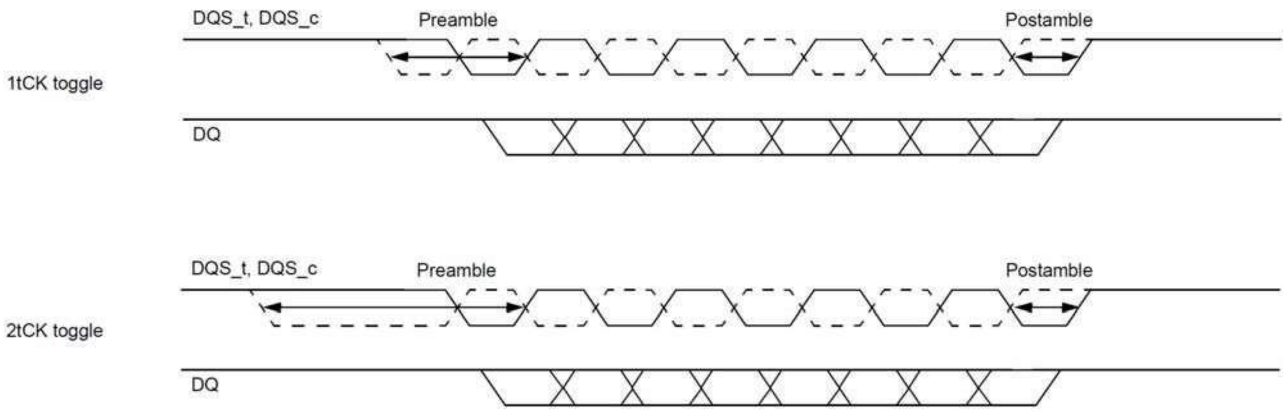
The DQS_t signal remains driven LOW and the DQS_c signal remains driven HIGH until an MPR Page0 READ command is issued (MPR0 through MPR3 determine which pattern is used), and when CAS latency (CL) has expired, the DQS signals will toggle normally depending on the burst length setting. To exit READ preamble training mode, an MRS command must be issued, MR4[A10] = 0.



Postamble

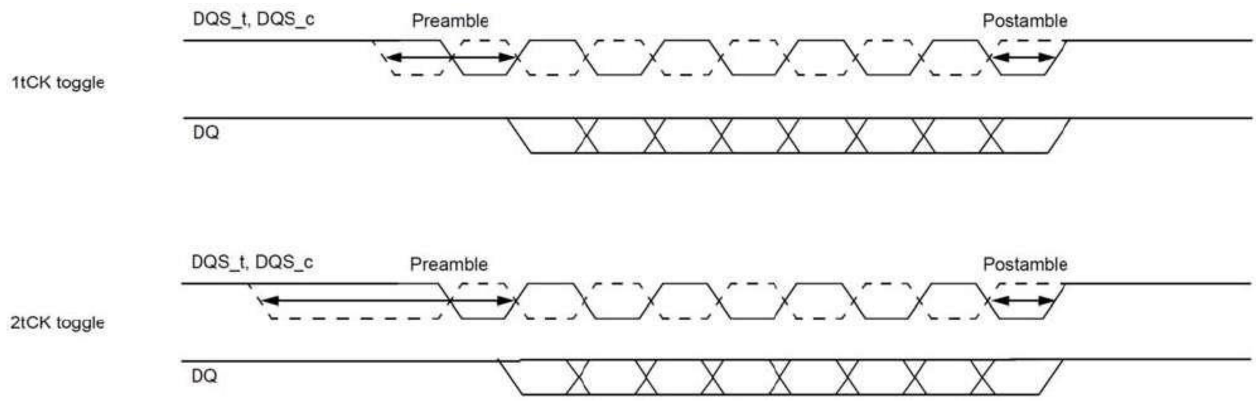
Write Postamble

DDR4 supports a fixed Write postamble. Write postamble nominal is 0.5tck for preamble modes 1tCK, 2tCK are shown below.



Read Postamble

DDR4 supports a fixed Read postamble. Read postamble nominal is 0.5tck for preamble modes 1tCK, 2tCK are shown below.



ACTIVATE Command

The ACTIVATE command is used to open (activate) a row in a particular bank for subsequent access. The values on the BG[1:0] inputs select the bank group, the BA[1:0] inputs select the bank within the bank group, and the address provided on inputs A[17:0] selects the row within the bank. This row remains active (open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

Bank-to-bank command timing for ACTIVATE commands uses two different timing parameters, depending on whether the banks are in the same or different bank group. tRRD_S (short) is used for timing between banks located in different bank groups. tRRD_L (long) is used for timing between banks located in the same bank group.

Another timing restriction for consecutive ACTIVATE commands [issued at tRRD (MIN)] is tFAW (fifth activate window). Because there is a maximum of four banks in a bank group, the tFAW parameter applies across different bank groups (five ACTIVATE commands issued at tRRD_L (MIN) to the same bank group would be limited by tRC).

Precharge Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation for a specified time (tRP) after the PRECHARGE command is issued. An exception to this is the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters.

After a bank is precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

The auto precharge feature is engaged when a READ or WRITE command is issued with A10 HIGH. The auto precharge feature uses the RAS lockout circuit to internally delay the PRECHARGE operation until the ARRAY RESTORE operation has completed. The RAS lockout circuit feature allows the PRECHARGE operation to be partially or completely hidden during burst READ cycles when the auto precharge feature is engaged. The PRECHARGE operation will not begin until after the last data of the burst write sequence is properly stored in the memory array.

Read Operation

READ Timing Definitions

Read timing shown below is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

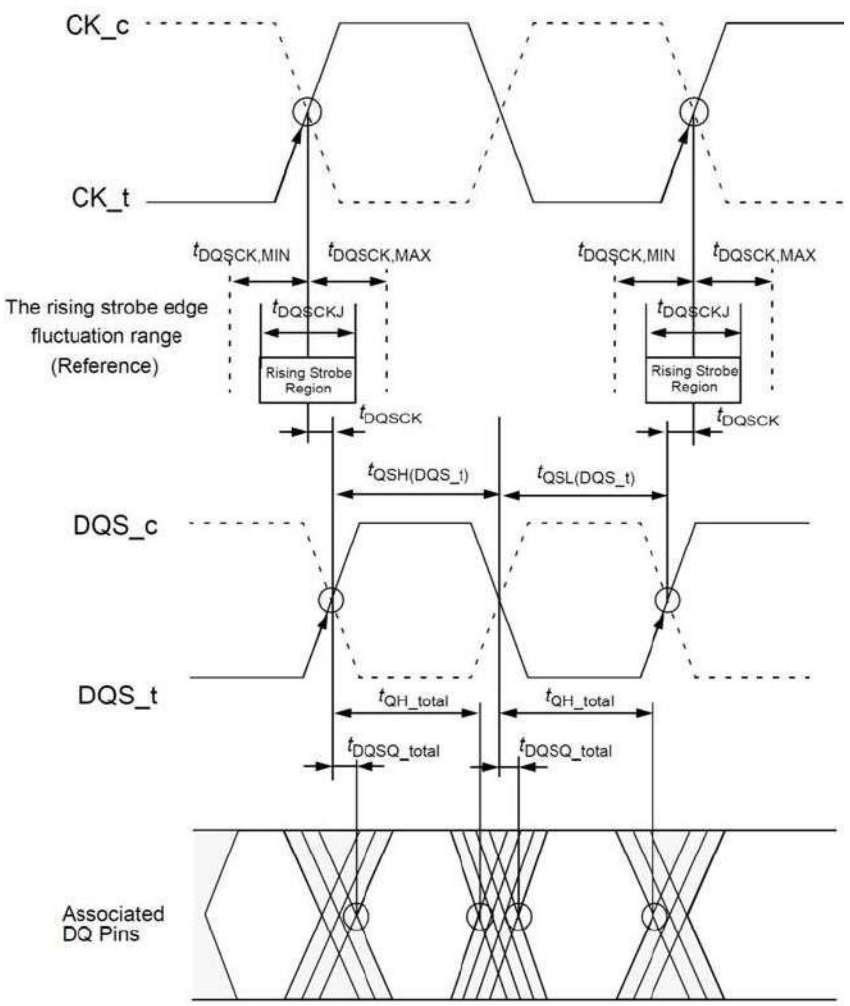
- tDQSCK (MIN)/(MAX) describes the allowed range for a rising data strobe edge relative to CK.
- tDQSCK is the actual position of a rising strobe edge relative to CK.
- tQSH describes the DQS differential output HIGH time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS differential output LOW time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ, both rising/falling edges of DQS, no tAC defined.

READ Timing Definition



READ Timing – Clock to Data Strobe Relationship

Clock to Data Strobe relationship is shown below6 and is applied when the DLL is enabled and locked.

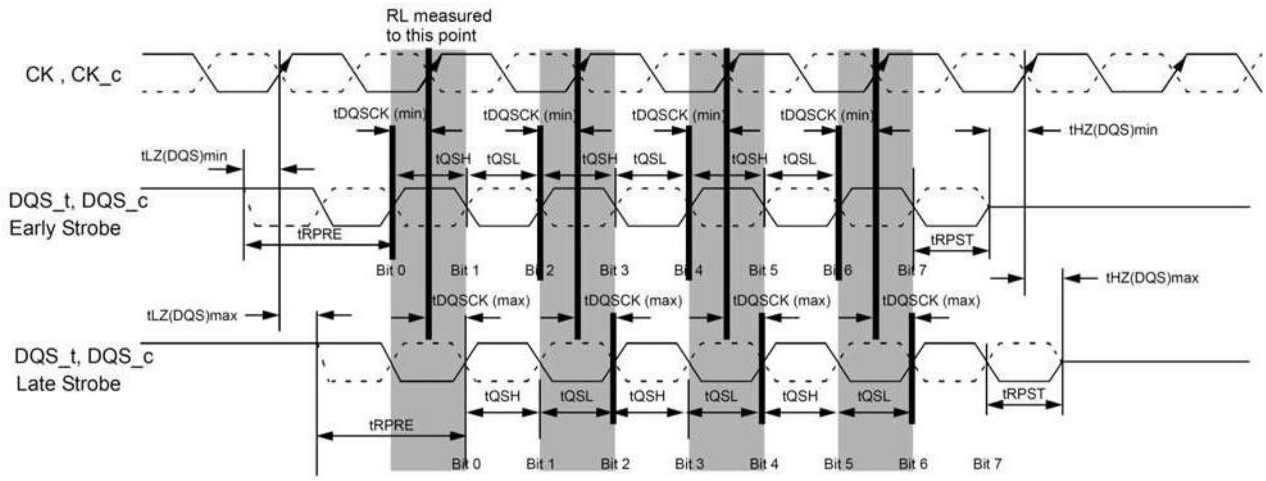
Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK_t, CK_c.
- tDQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS), tHZ(DQS) for preamble/postamble.

Clock to Data Strobe Relationship



NOTE

1. Within a burst, the rising strobe edge will vary within tDQSCKj while at the same voltage and temperature. However, when the device, voltage, and temperature variations are incorporated, the rising strobe edge variance window can shift between tDQSCK (MIN) and tDQSCK (MAX).

   A timing of this window's right edge (latest) from rising CK_t, CK_c is limited by a device's actual tDQSCK (MAX). A timing of this window's left inside edge (earliest) from rising CK_t, CK_c is limited by tDQSCK (MIN).
2. Notwithstanding Note 1, a rising strobe edge with tDQSCK (MAX) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK (MIN) at T(n + 1) because other timing relationships (tQSH, tQSL) exist: if tDQSCK(n + 1) < 0: tDQSCK(n) < 1.0 tCK - (tQSH (MIN) + tQSL (MIN)) - | tDQSCK(n + 1) |.
3. The DQS_t, DQS_c differential output HIGH time is defined by tQSH, and the DQS_t, DQS_c differential output LOW time is defined by tQSL.
4. tLZ(DQS) MIN and tHZ(DQS) MIN are not tied to tDQSCK (MIN) (early strobe case), and tLZ(DQS) MAX and tHZ(DQS) MAX are not tied to tDQSCK (MAX) (late strobe case).
5. The minimum pulse width of READ preamble is defined by tRPRE (MIN).
6. The maximum READ postamble is bound by tDQSCK (MIN) plus tQSH (MIN) on the left side and tHZDSQ (MAX) on the right side.
7. The minimum pulse width of READ postamble is defined by tRPST (MIN).
8. The maximum READ preamble is bound by tLZDQS (MIN) on the left side and tDQSCK (MAX) on the right side.

READ Timing – Data Strobe to Data Relationship

The data strobe to data relationship is shown below and is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

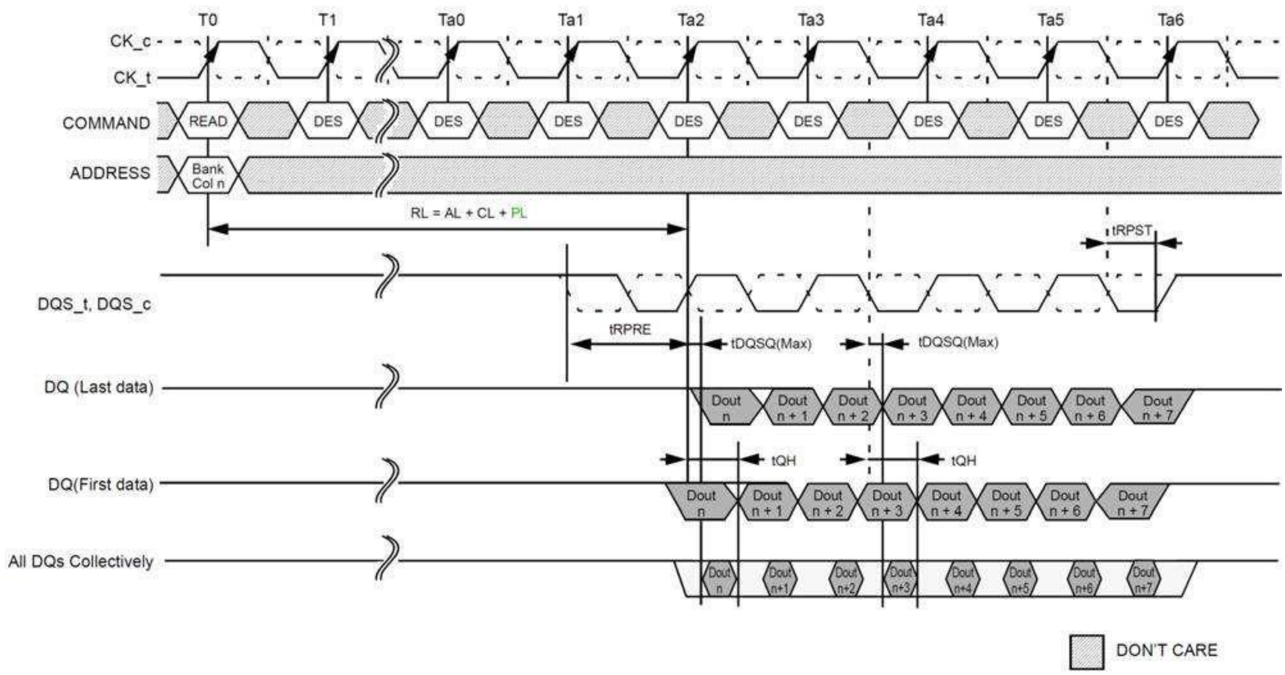
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

Data Strobe to Data Relationship



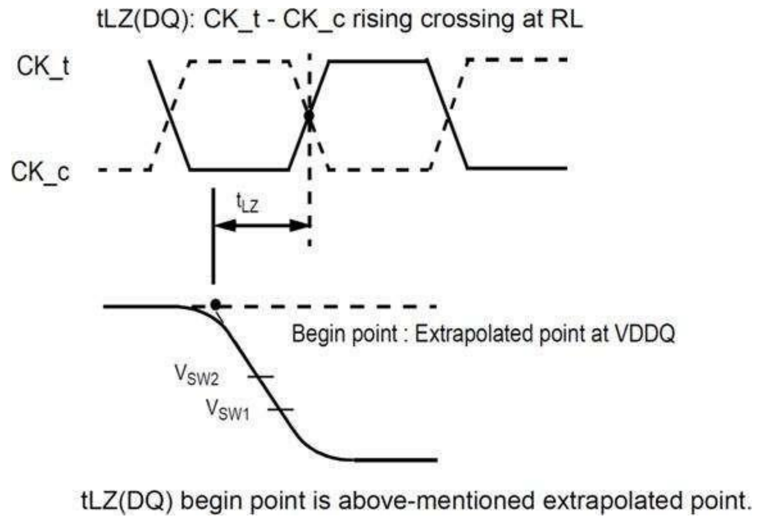
NOTE

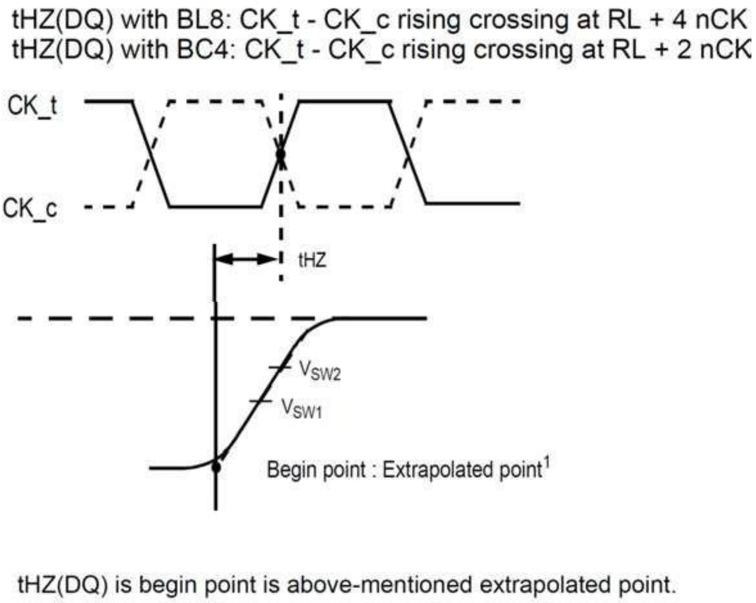
1. BL = 8, RL = 11 (AL = 0, CL = 1) , Premable = 1tCK.
2. DOUT*n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0.
5. Output timings are referenced to VDDQ, and DLL on for locking.
6. tDQSQ defines the skew between DQS to data and does not define DQS to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) and tLZ(DQ). The figure below shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS) and tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled-ended parameters.

tLZ and tHZ method for calculating transitions and begin points



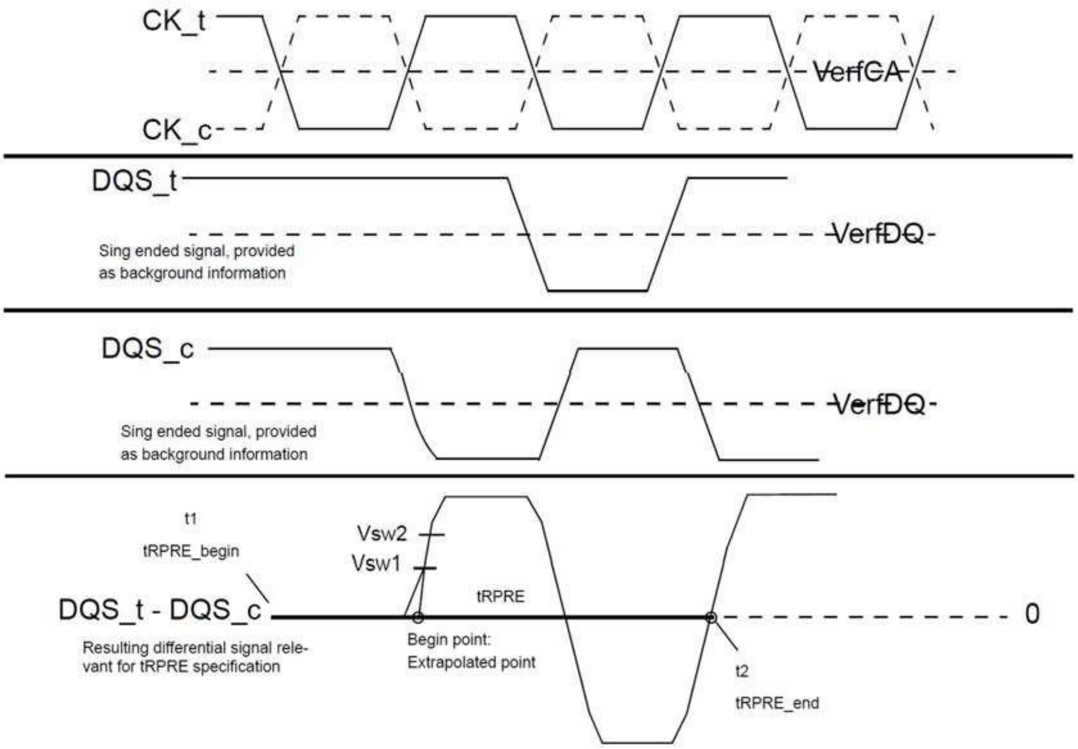


NOTE

1. Vsw1 = (0.70 - 0.04) × VDDQ for both tLZ and tHZ.
2. Vsw2 = (0.70 + 0.04) × VDDQ for both tLZ and tHZ.
3. Extrapolated point (low level) = VDDQ/(50 + 34) × 34 = 0.4 × VDDQ
   Driver impedance = RZQ/7 = 34ohm
   VTT test load = 50ohm to VDDQ.

tRPRE Calculation

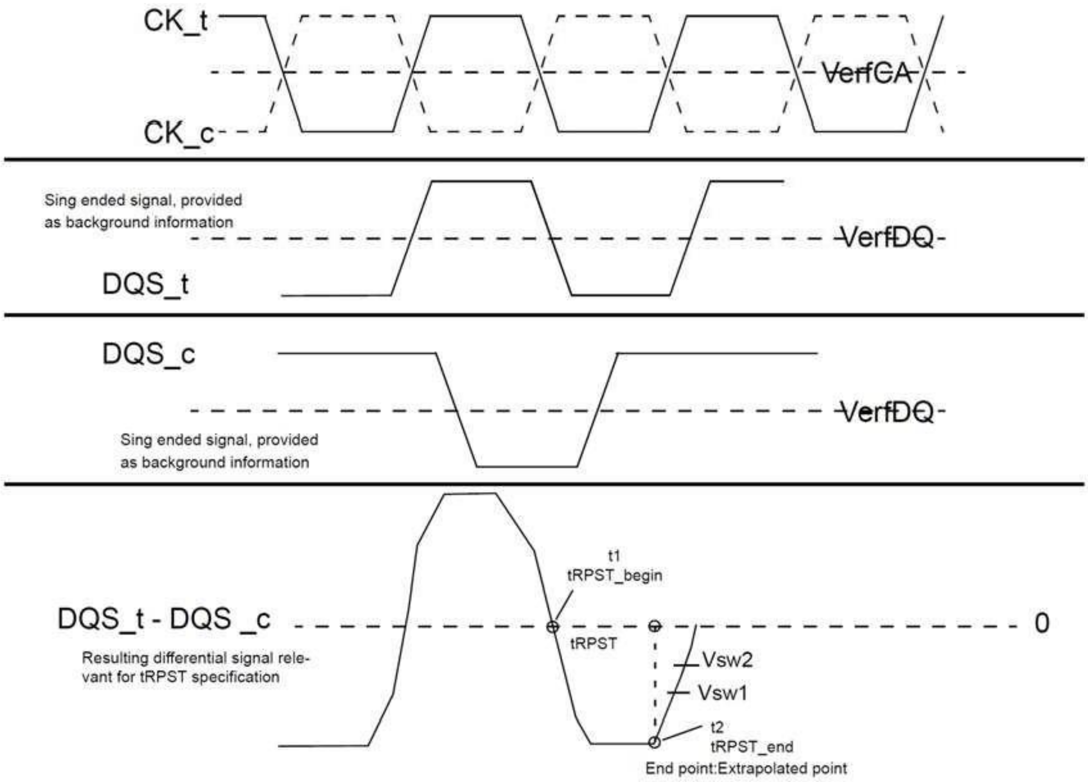
Method for Calculating tRPRE Transitions and Endpoints



NOTE
1. Vsw1 = (0.3 - 0.04) × VDDQ.
2. Vsw2 = (0.30 + 0.04) × VDDQ.
3. DQS_t and DQS_c low level = VDDQ/(50 + 34) × 34 = 0.4 × VDDQ
   Driver impedance = RZQ/7 = 34ohm
   VTT test load = 50ohm to VDDQ.

tRPST Calculation

tRPST Method for Calculating Transitions and Endpoints



NOTE

1. Vsw1 = (–0.3 - 0.04) × VDDQ.
2. Vsw2 = (–0.30 + 0.04) × VDDQ.
3. DQS_t and DQS_c low level = VDDQ/(50 + 34) × 34 = 0.4 × VDDQ
   Driver impedance = RZQ/7 = 34ohm
   VTT test load = 50ohm to VDDQ.

READ Burst Operation

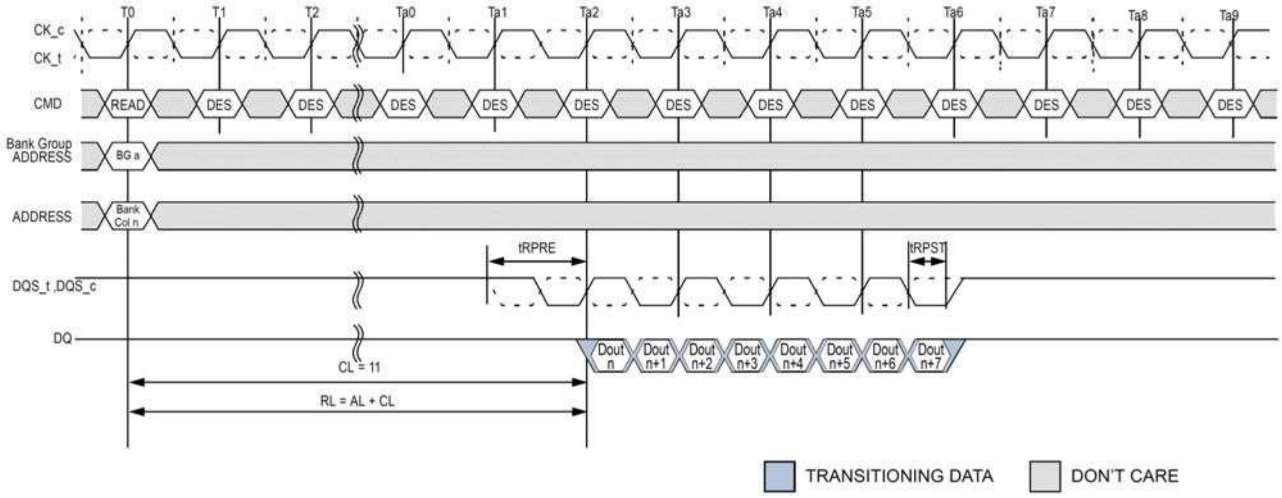
DDR4 READ commands support bursts of BL8 (fixed), BC4 (fixed), and BL8/BC4 on-the-fly (OTF); OTF uses address A12 to control OTF when OTF is enabled:

- A12 = 0, BC4 (BC4 = burst chop)
- A12 = 1, BL8

READ commands can issue precharge automatically with a READ with auto precharge command (RDA), and is enabled by A10 HIGH:

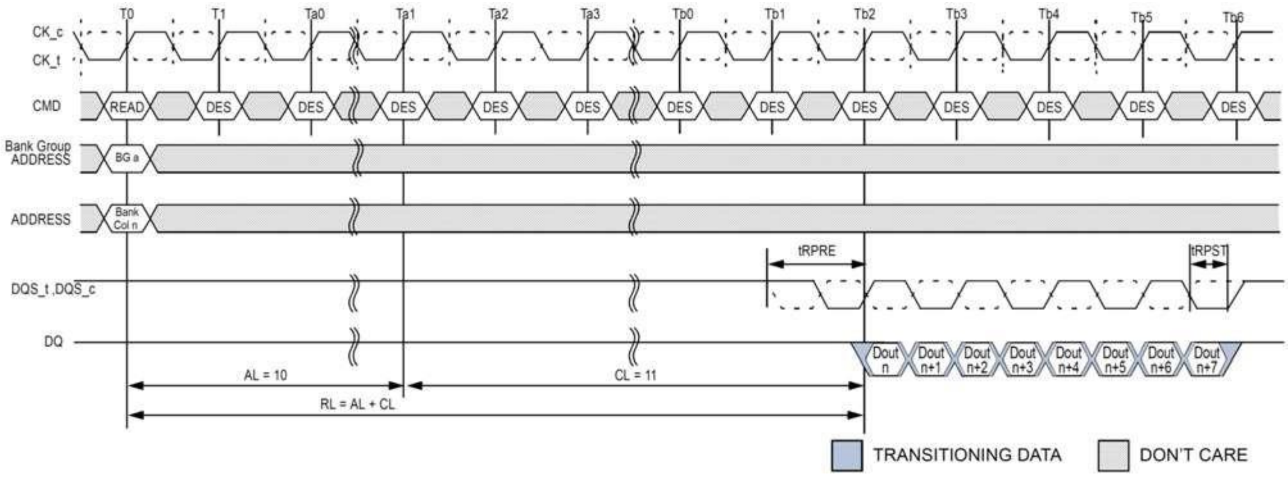
- READ command with A10 = 0 (RD) performs standard read, bank remains active after READ burst.
- READ command with A10 = 1 (RDA) performs read with auto precharge, bank goes in to precharge after READ burst.

READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



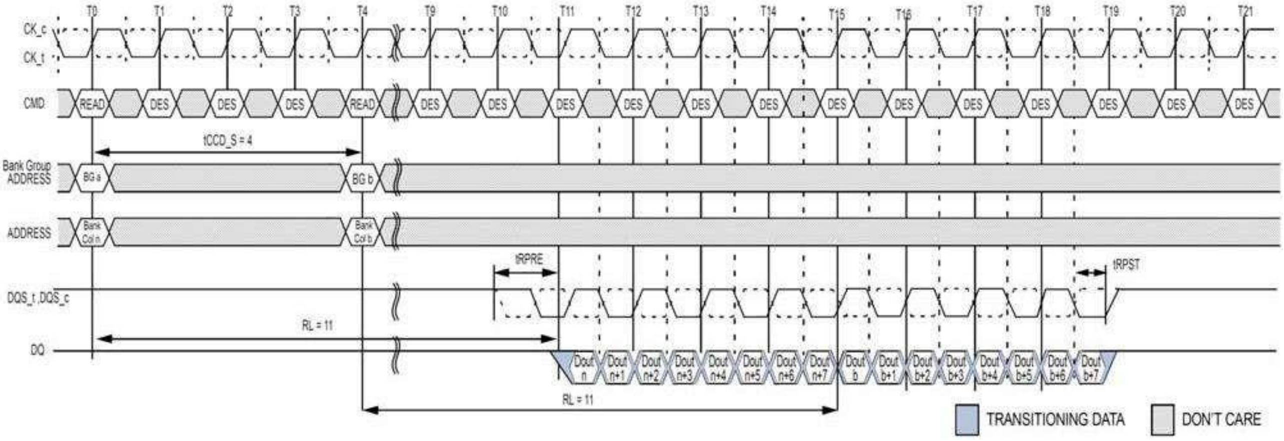
NOTE
1. BL8, RL = 0, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



NOTE
1. BL8, RL = 21, AL = (CL - 1), CL = 11, Preamble = 1tCK.
2. DO *n* = data-out from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

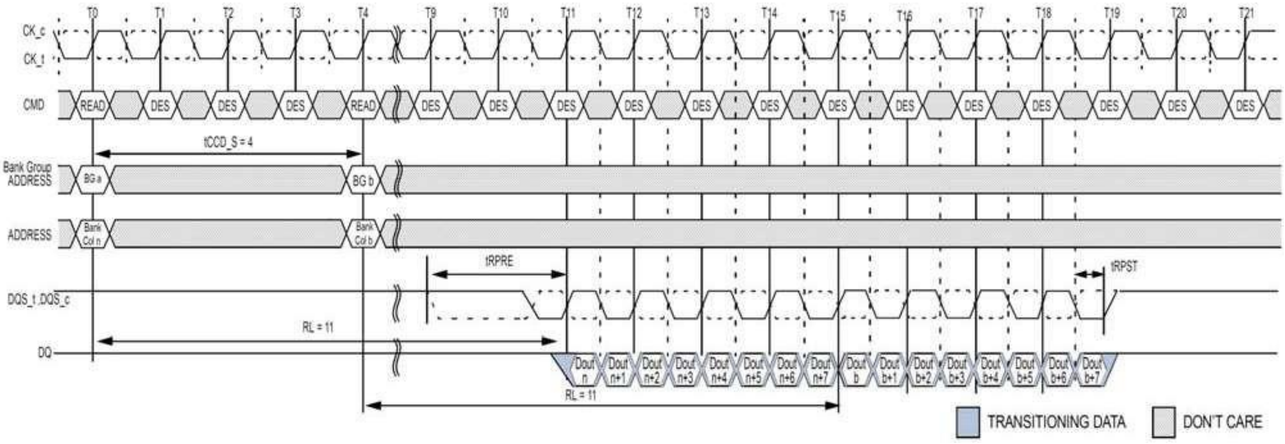
Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



NOTE

1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READcommands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

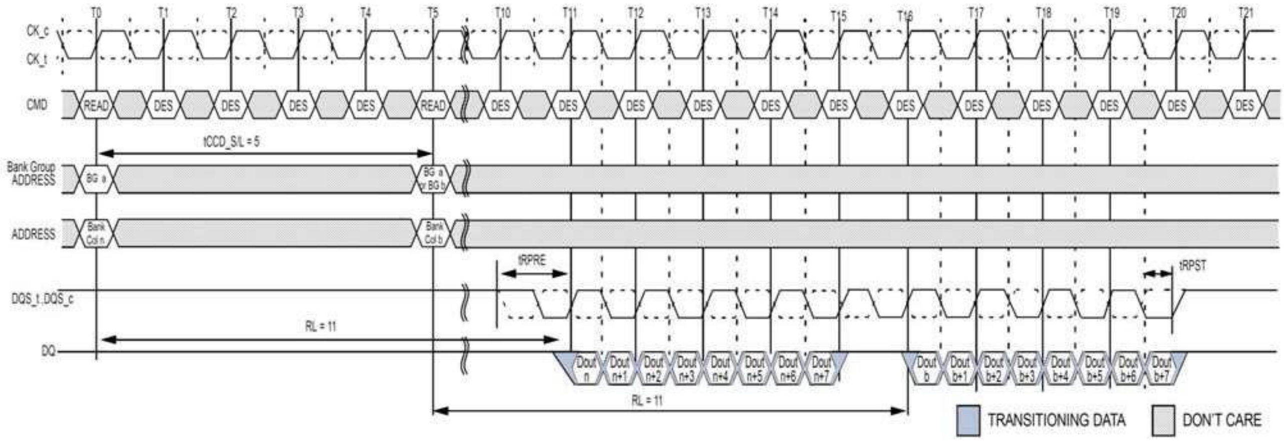
Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



NOTE

1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

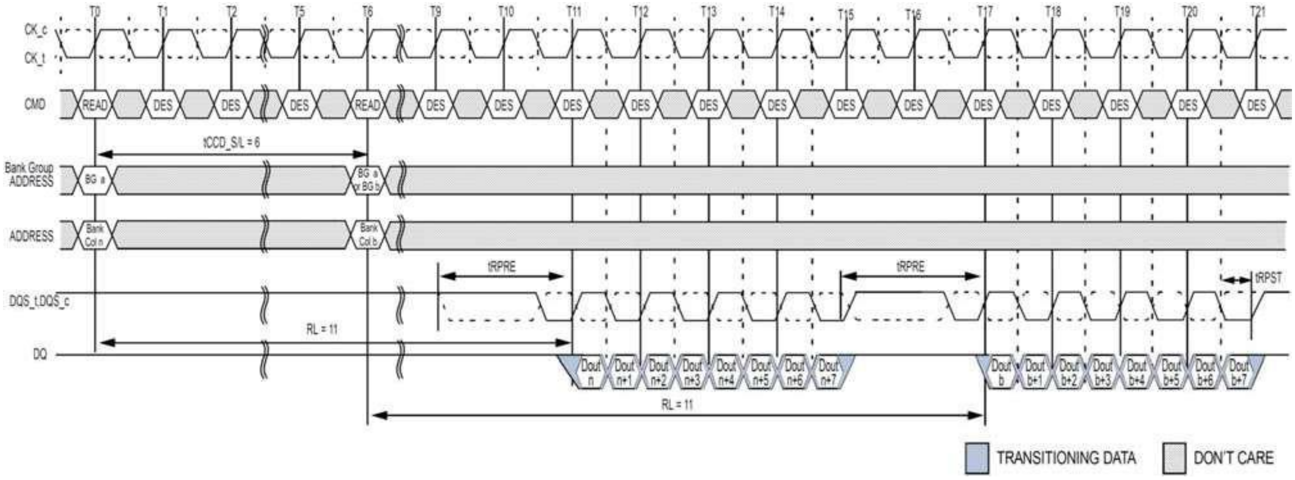
Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE

1. BL8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ commands at T0 and T5.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

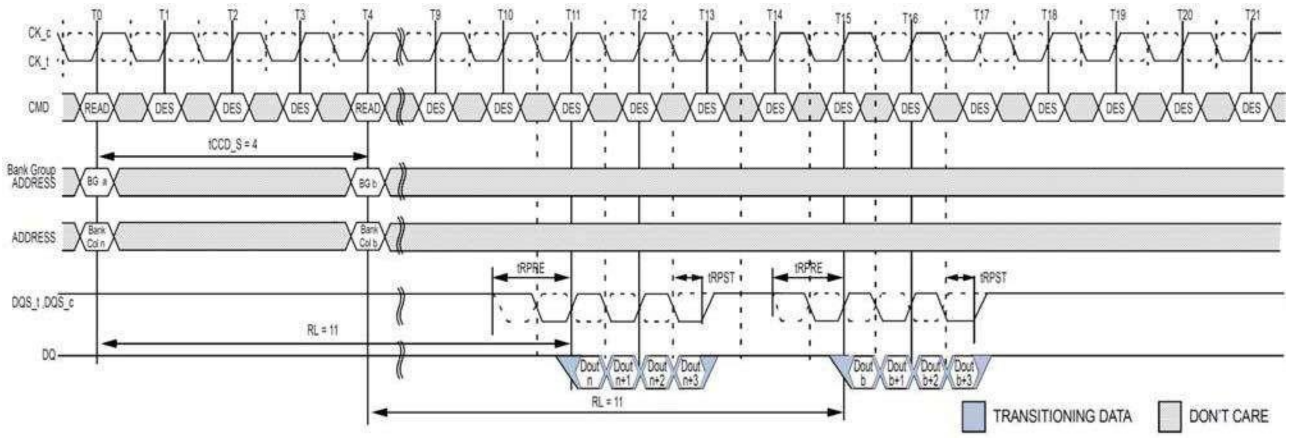
Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE

1. BL8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ commands at T0 and T6.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.
6. tCCD_S/L = 5 isn't allowed in 2tCK preamble mode.

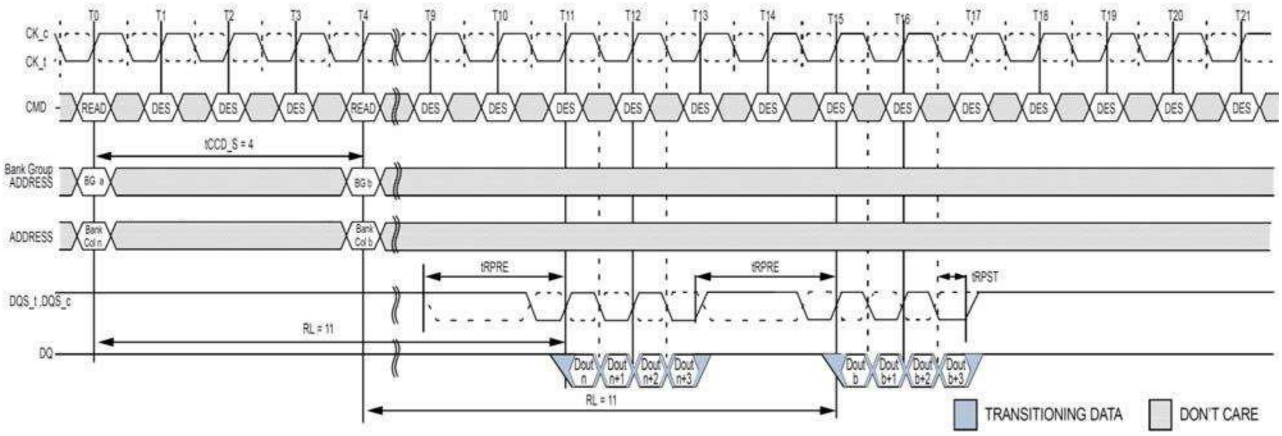
READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



NOTE

1. BL8, AL = 0, CL = 11, Preamble = 1tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

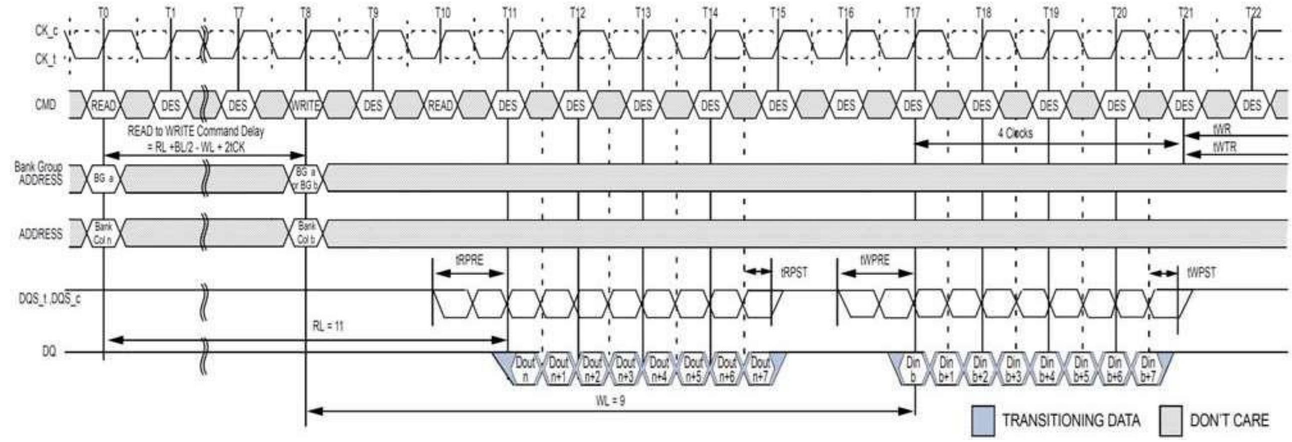
READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



NOTE

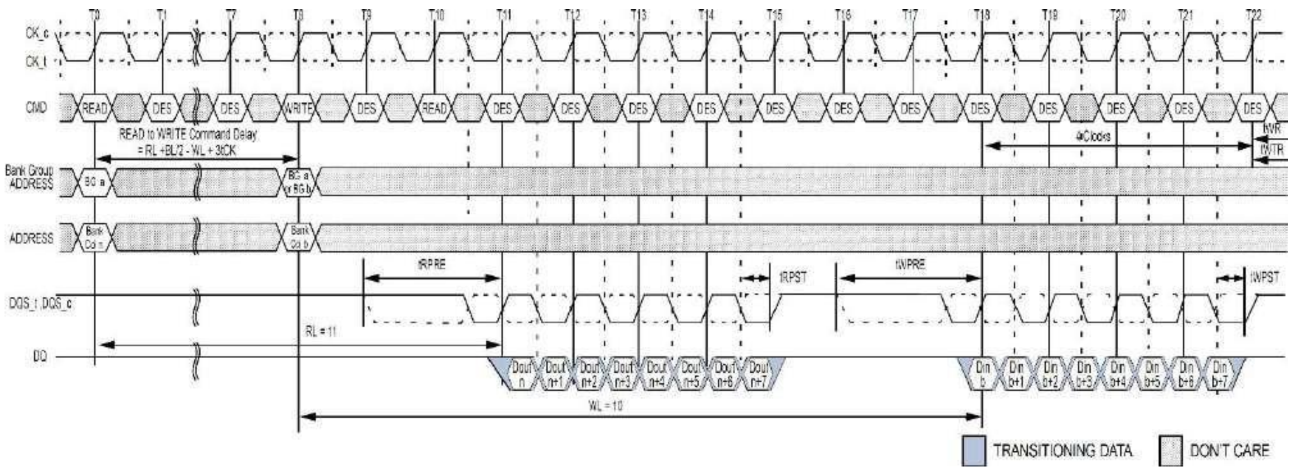
1. BL8, AL = 0, CL = 11, Preamble = 2tCK.
2. DO *n* (or *b*) = data-out from column *n* (or column *b*).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ commands at T0 and T4.
5. CA parity = Disable, CS to CA latency = Disable, Read DBI = Disable.

READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



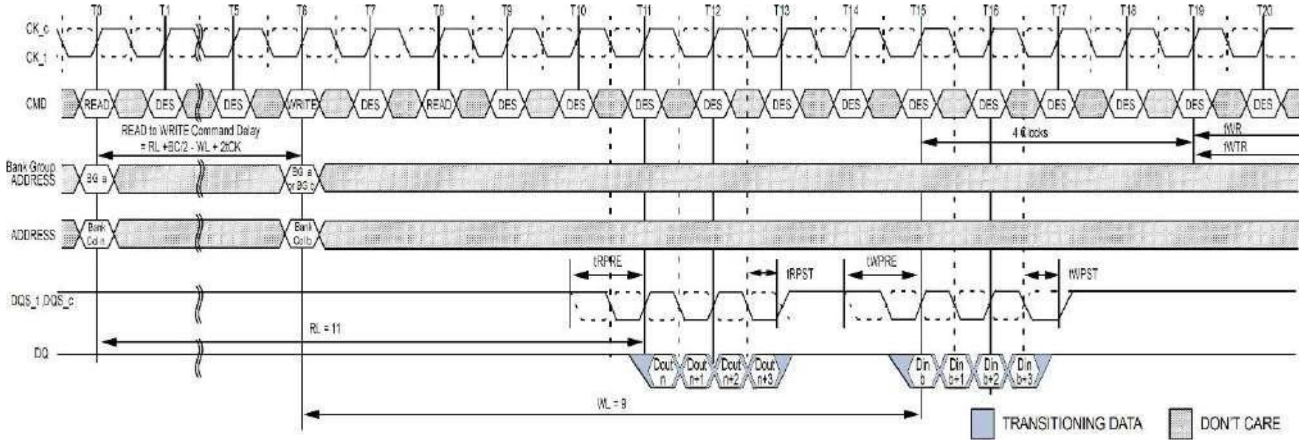
NOTE
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0 A[1:0] = 00 or MR0 A[1:0] = 01and A12 = 1 during READ command at T0 and WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



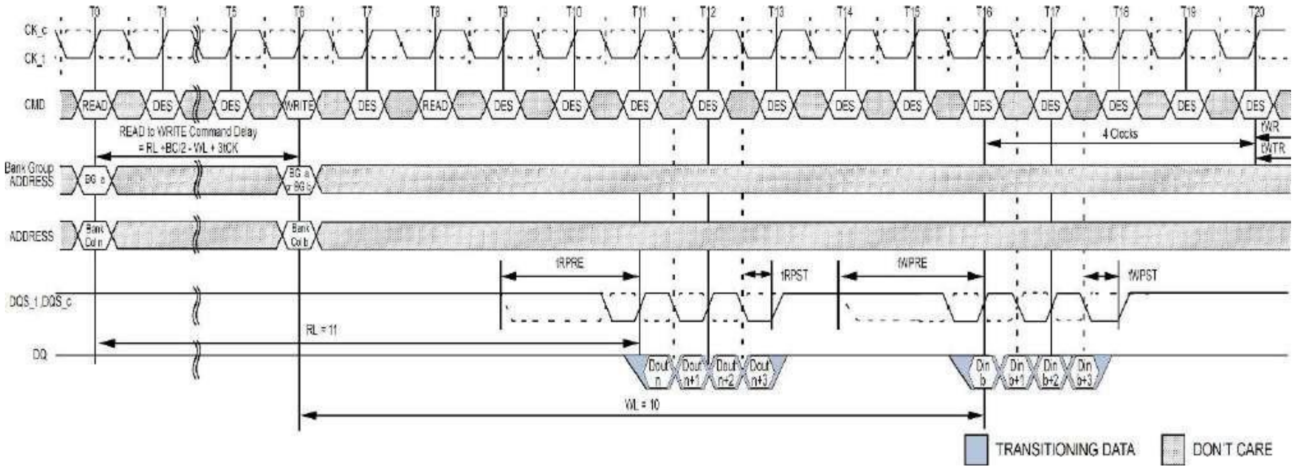
NOTE
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



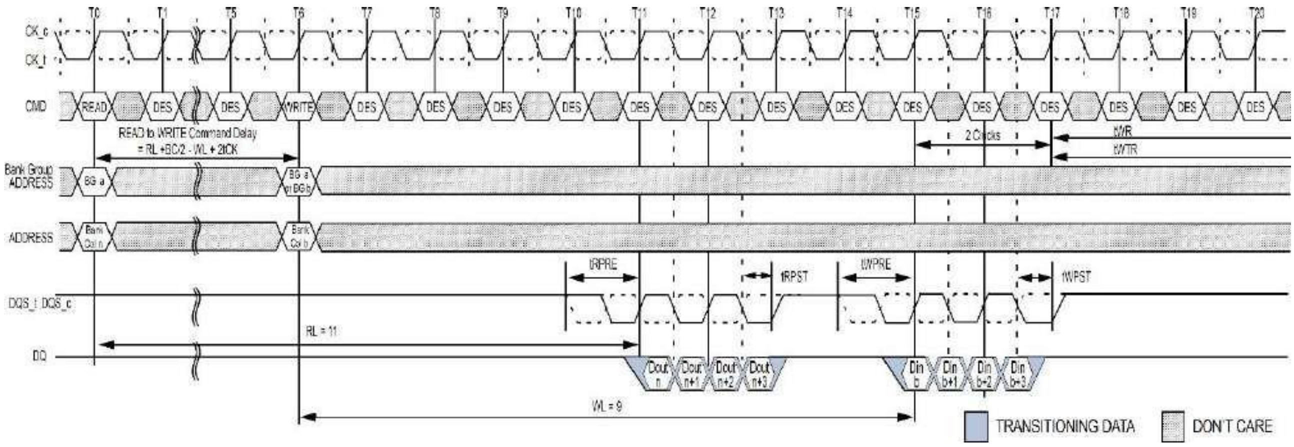
NOTE
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



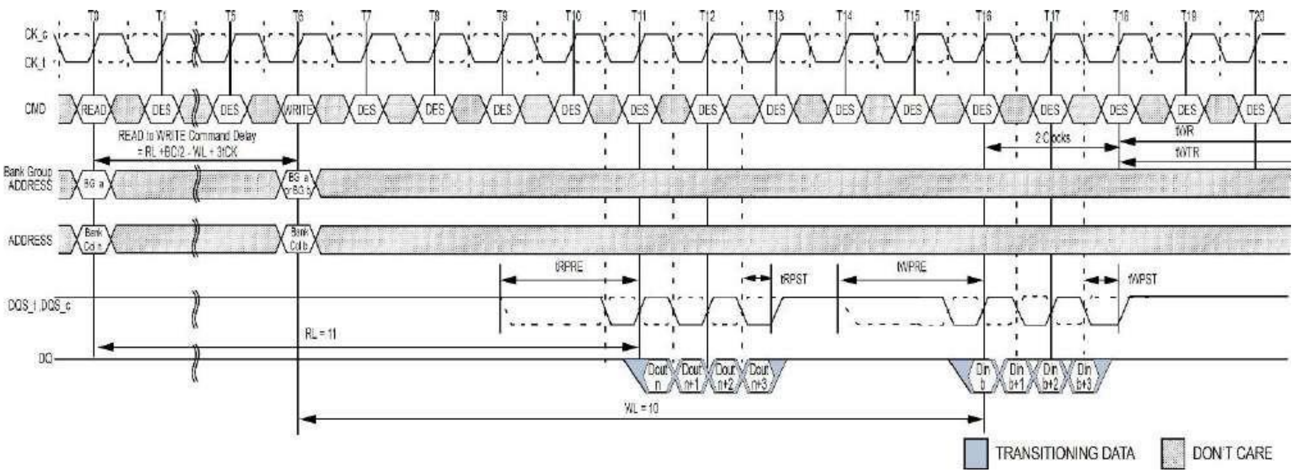
NOTE
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



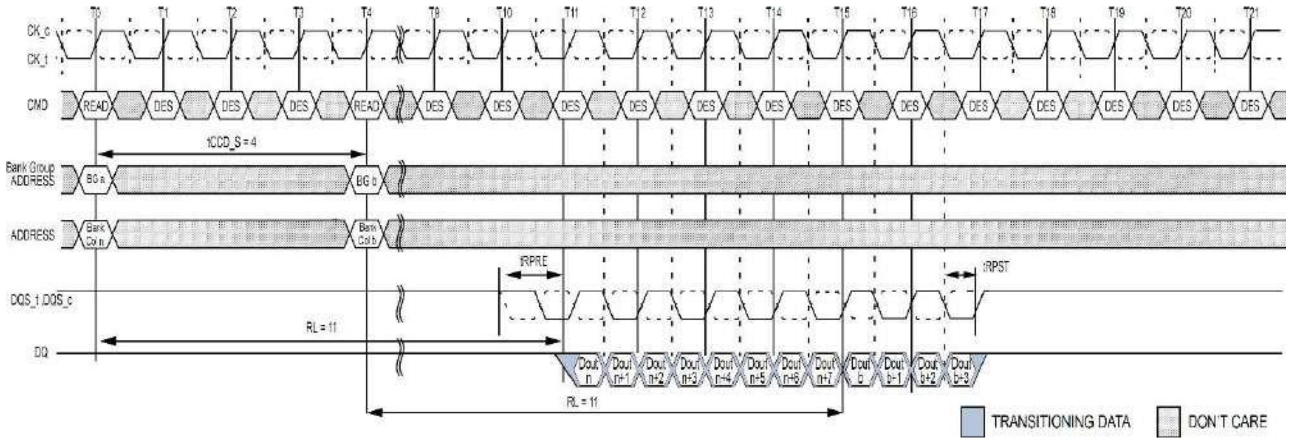
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



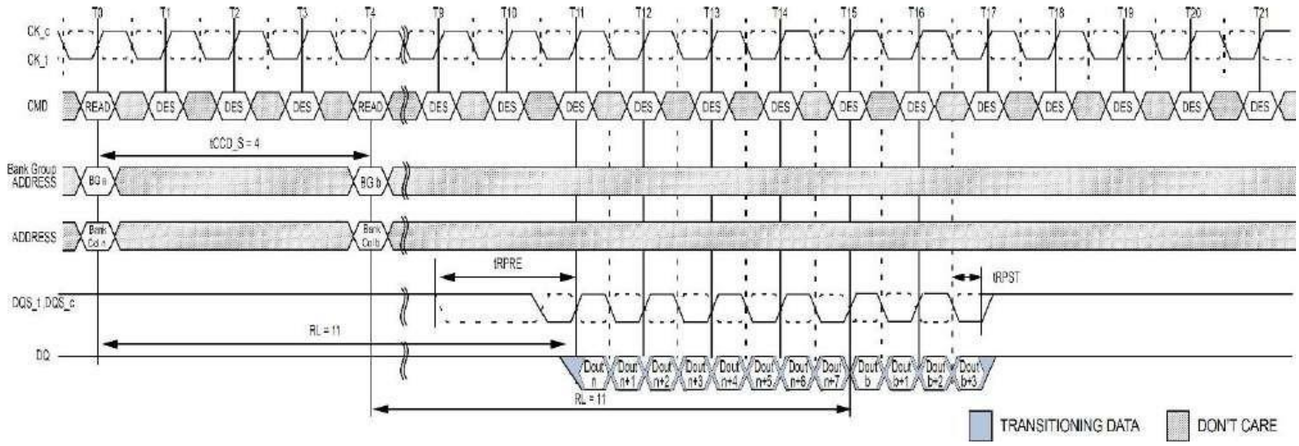
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



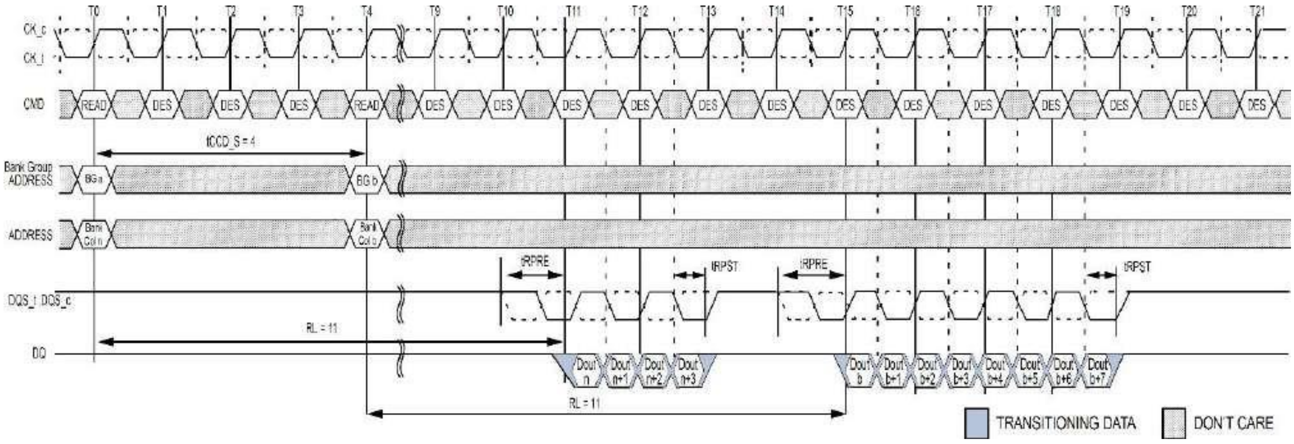
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

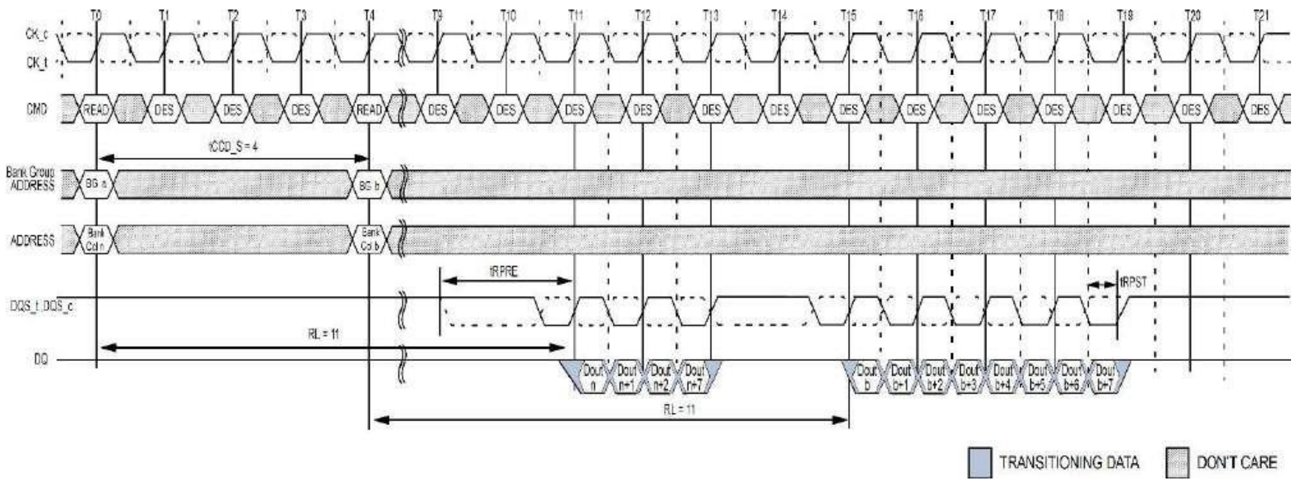
READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



NOTE :

1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

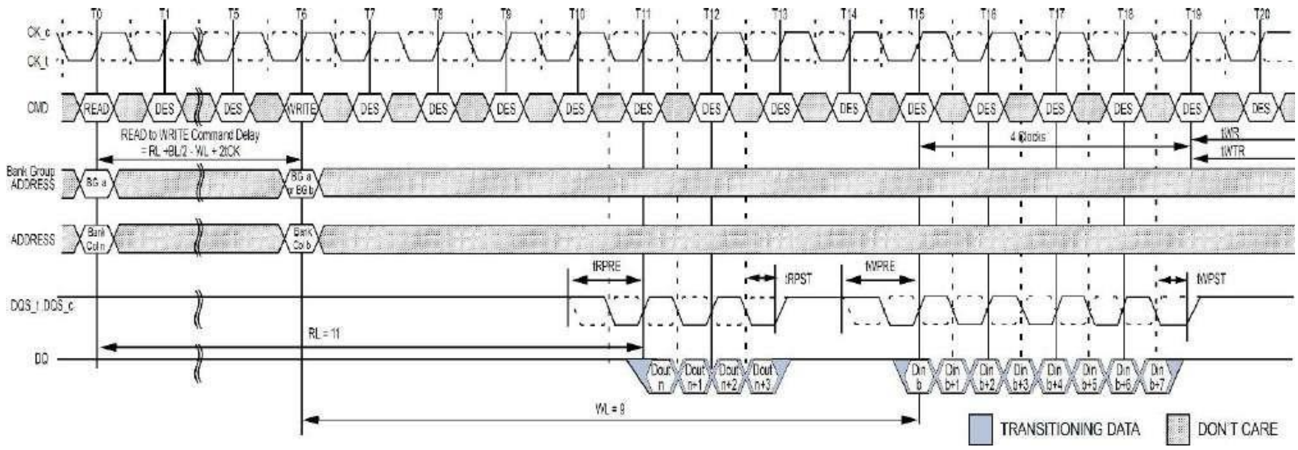
READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



NOTE :

1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

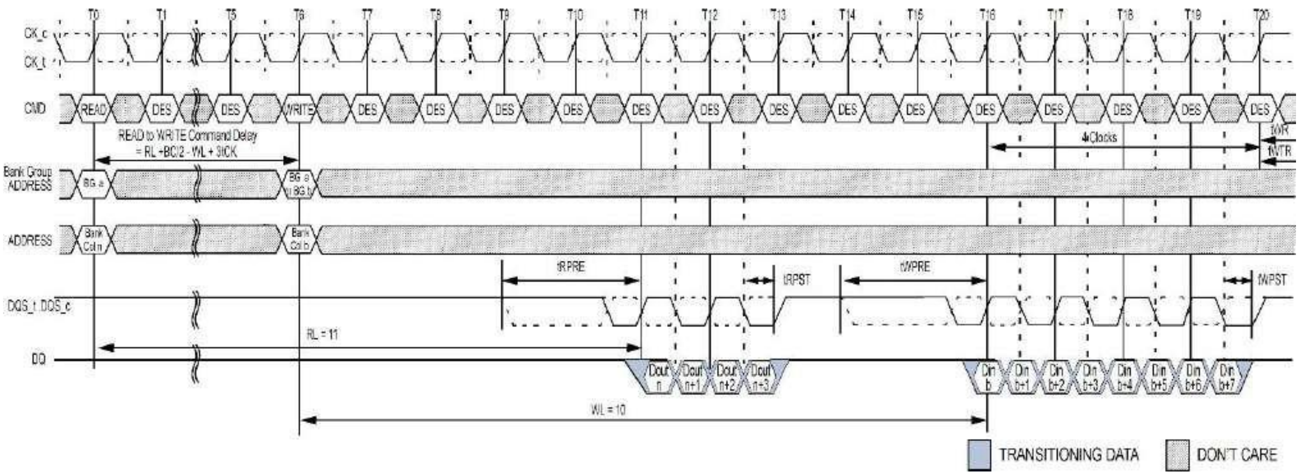
READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE :

1. BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

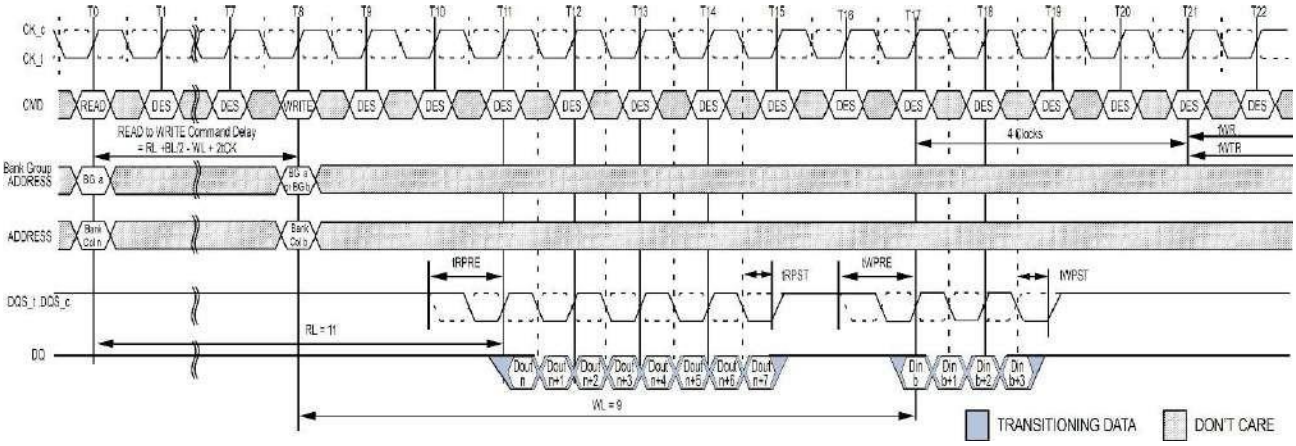
READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE :

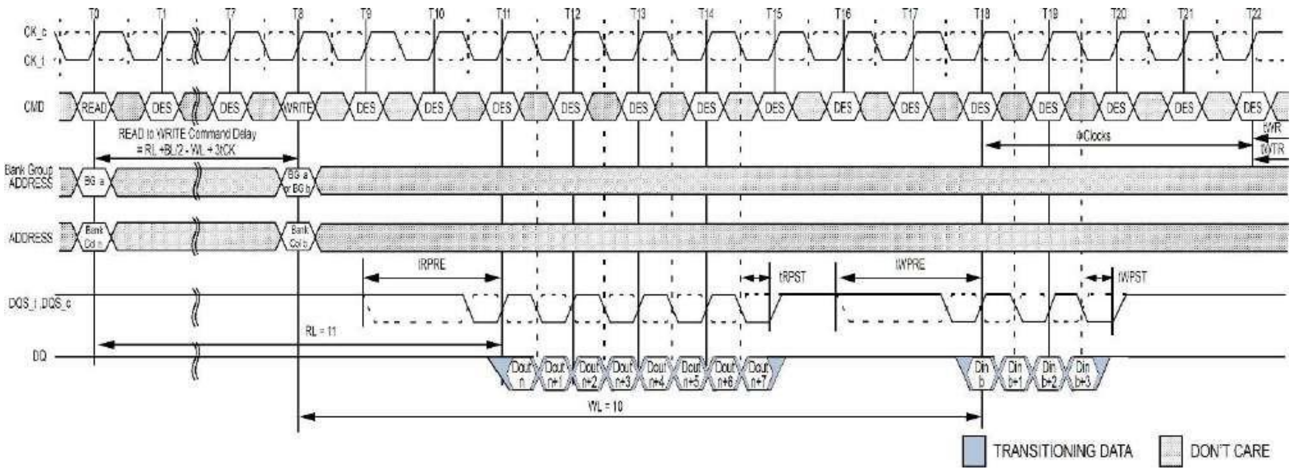
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1*5, AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

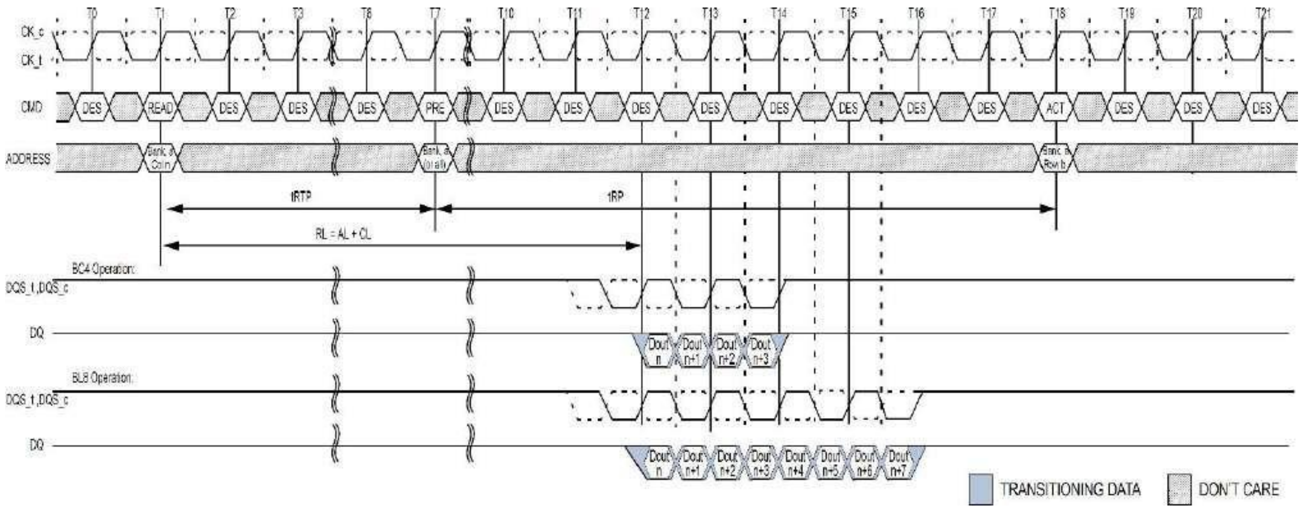
Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given bytRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in READ to PRECHARGE with 1tCK Preamble to READ to PRECHARGE with Additive Latency and 1tCK Preamble.

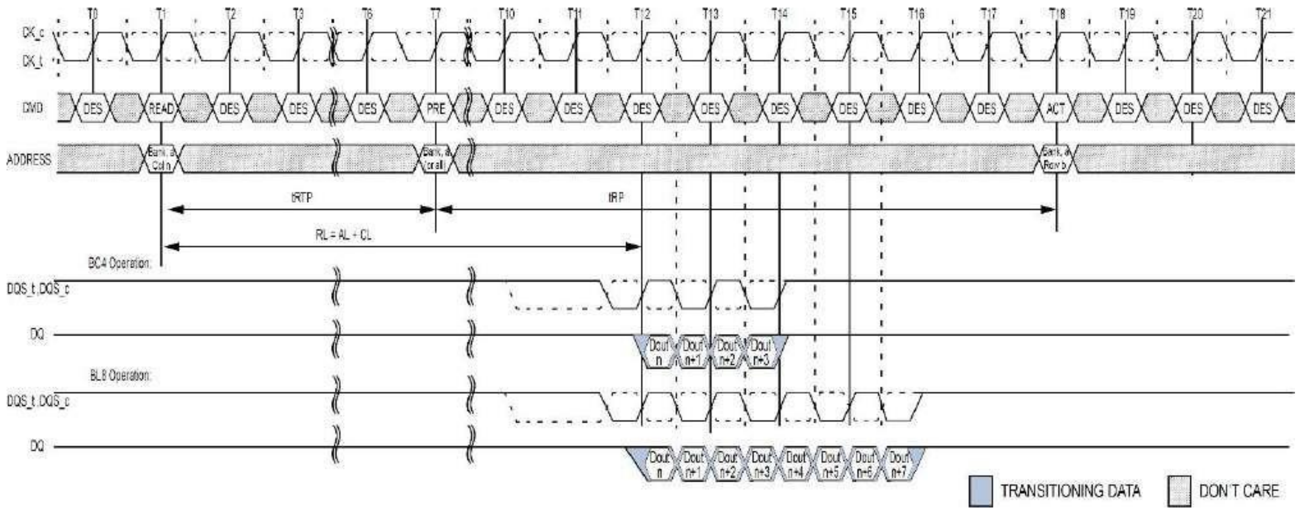
READ to PRECHARGE with 1tCK Preamble



NOTE :

1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

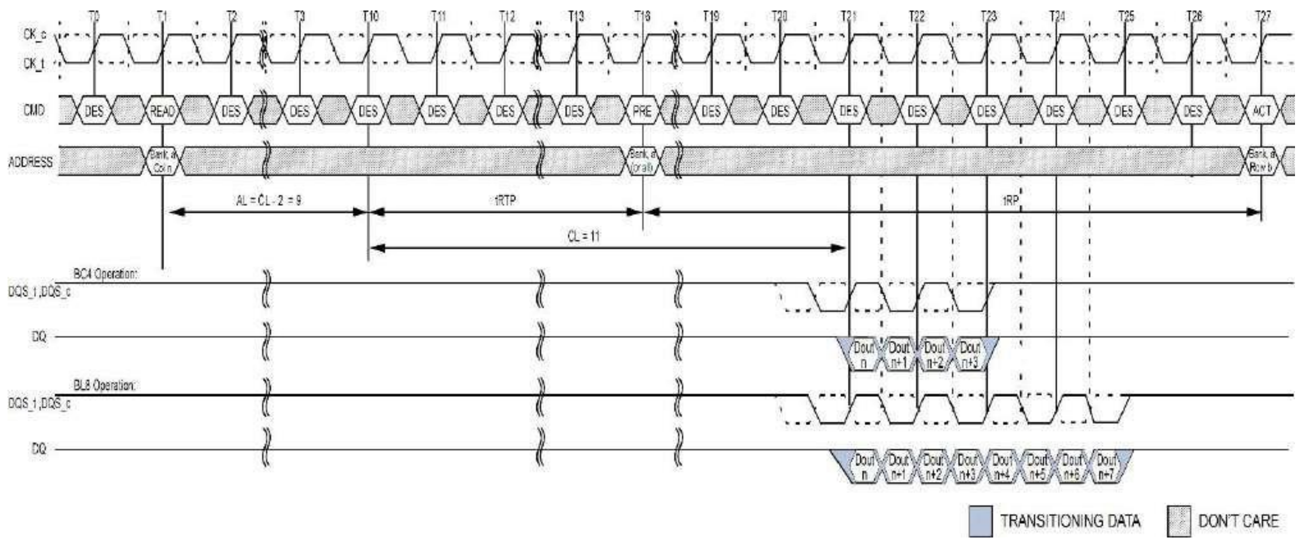
READ to PRECHARGE with 2tCK Preamble



NOTE :

1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

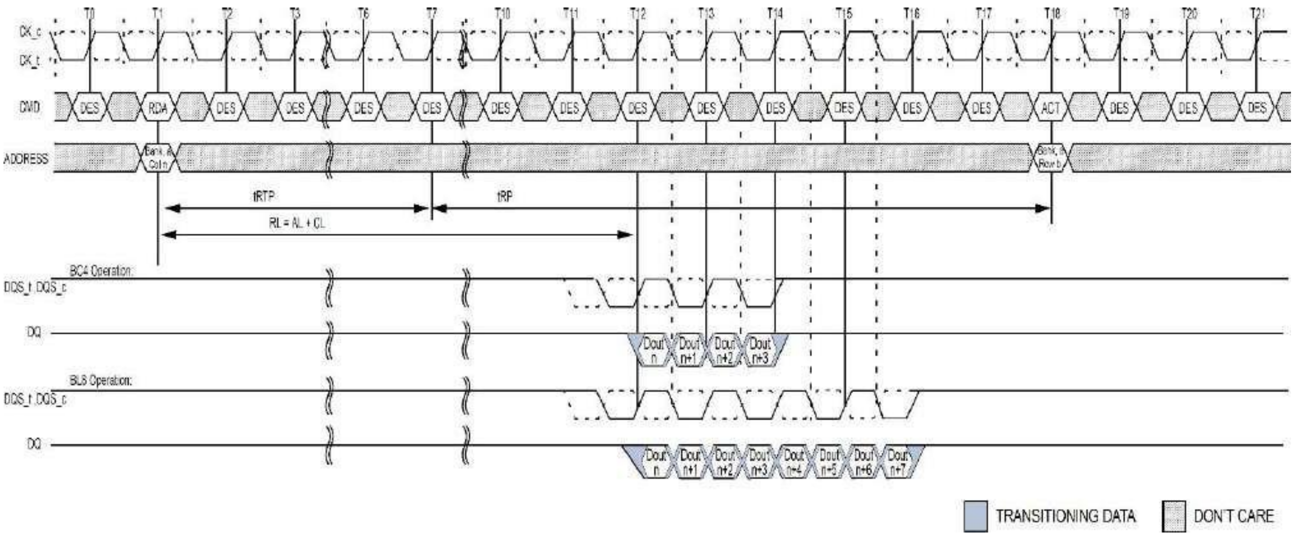
READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE :

1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

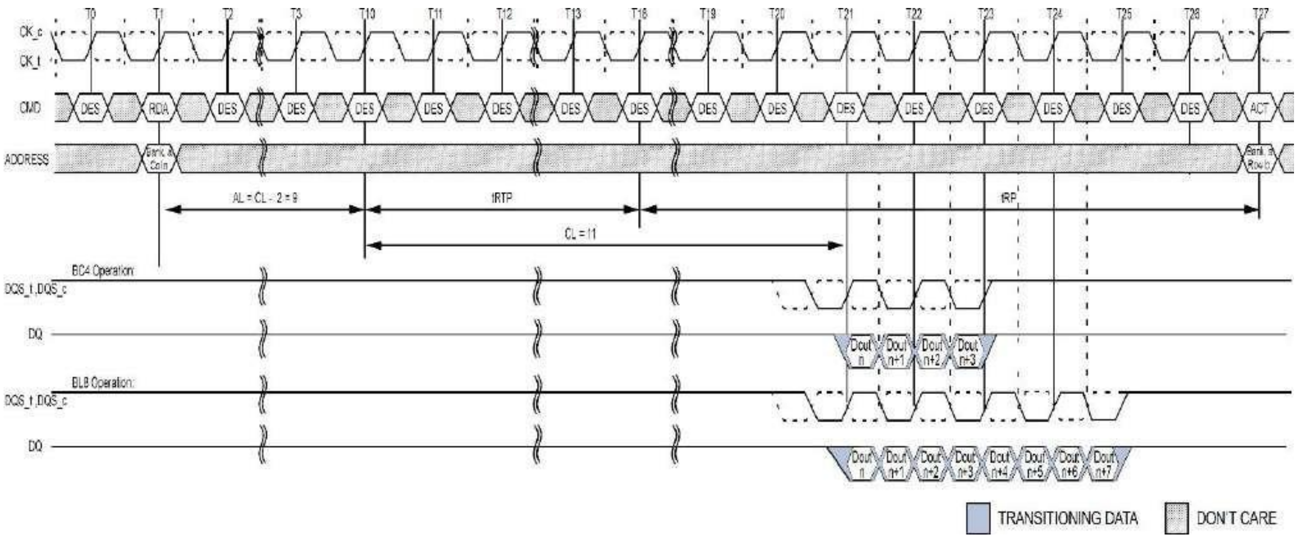
READ with Auto Precharge and 1tCK Preamble



NOTE :

1. BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T18).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

READ with Auto Precharge, Additive Latency and 1tCK Preamble

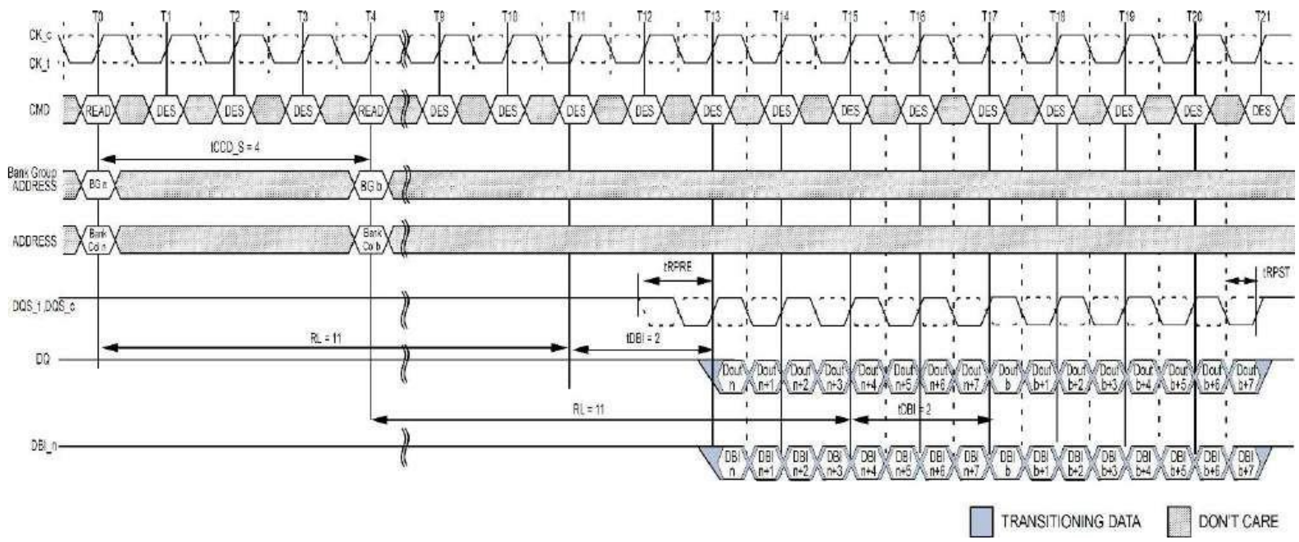


NOTE :

1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T27).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Burst Read Operation with Read DBI (Data Bus Inversion)

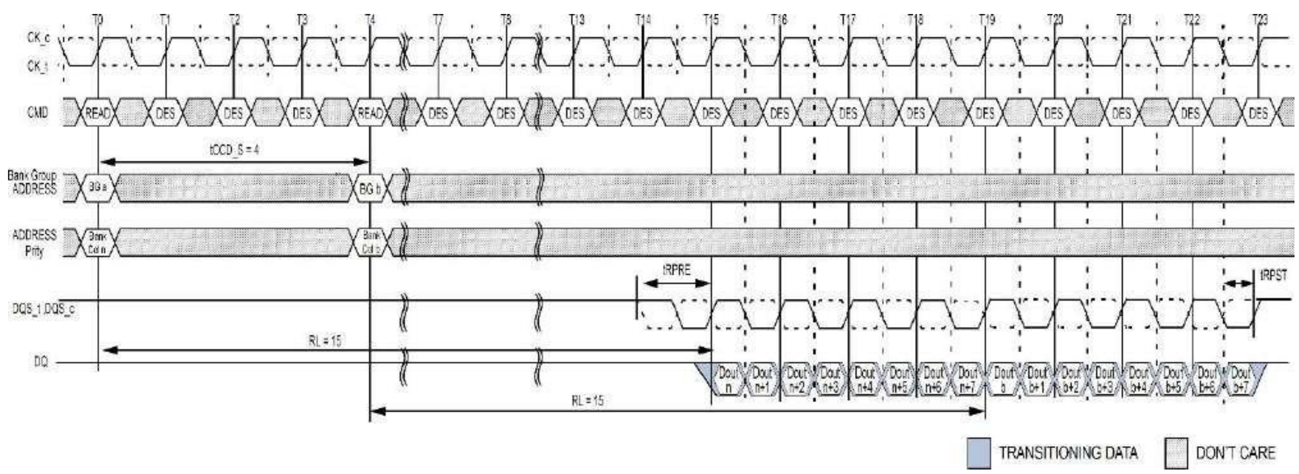
Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group



NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustrat:ion; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

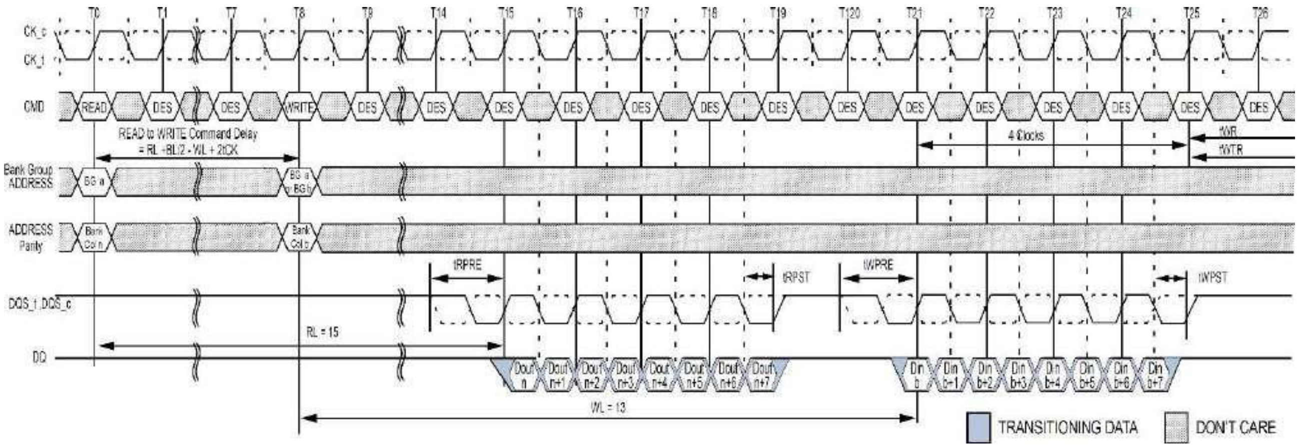
Burst Read Operation with Command/Address Parity

Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE :
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity =Enable, CS to CA Latency = Disable, Read DBI = Disable.

READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group

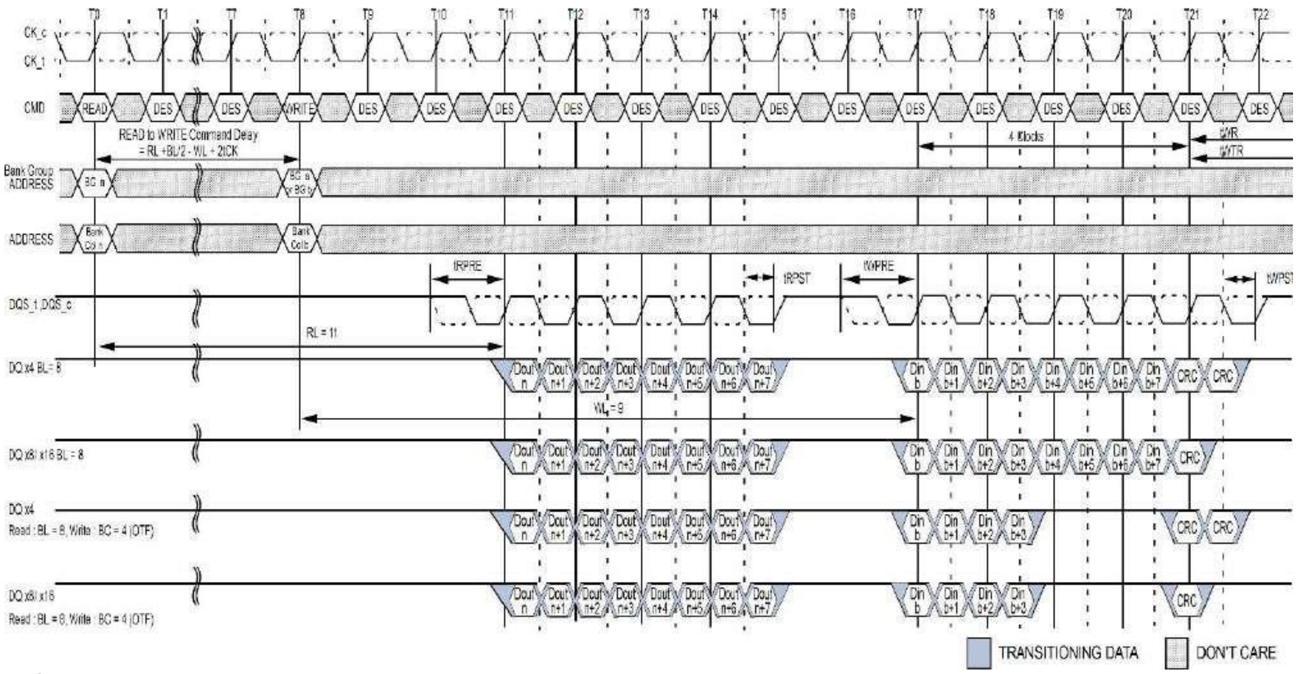


NOTE :

1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CL+AL+PL=13), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

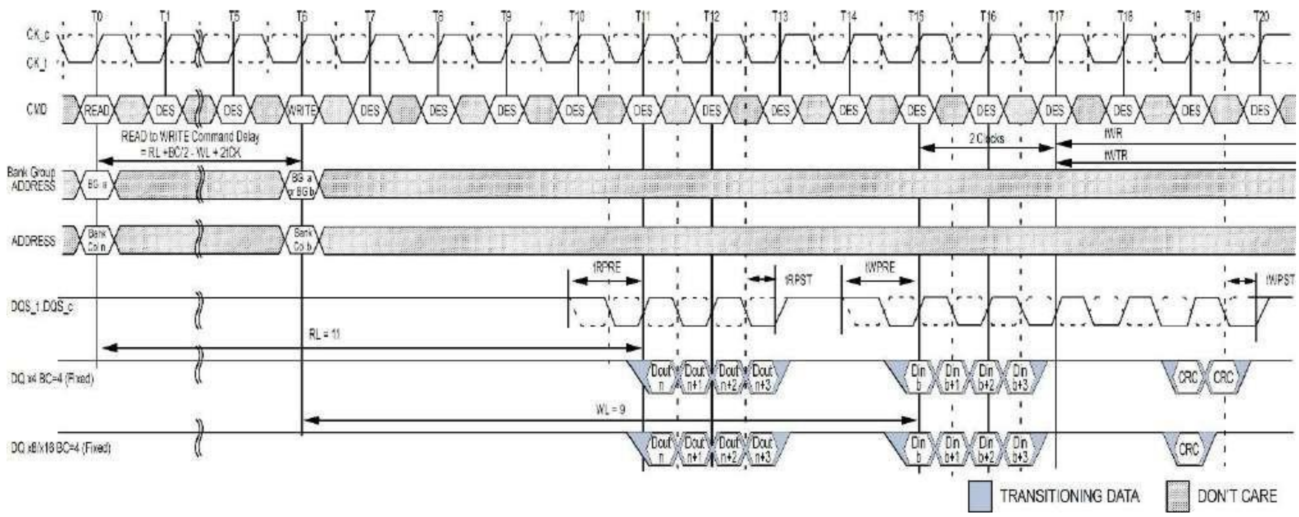
Read to Write with Write CRC

READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE :
1. BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble= 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

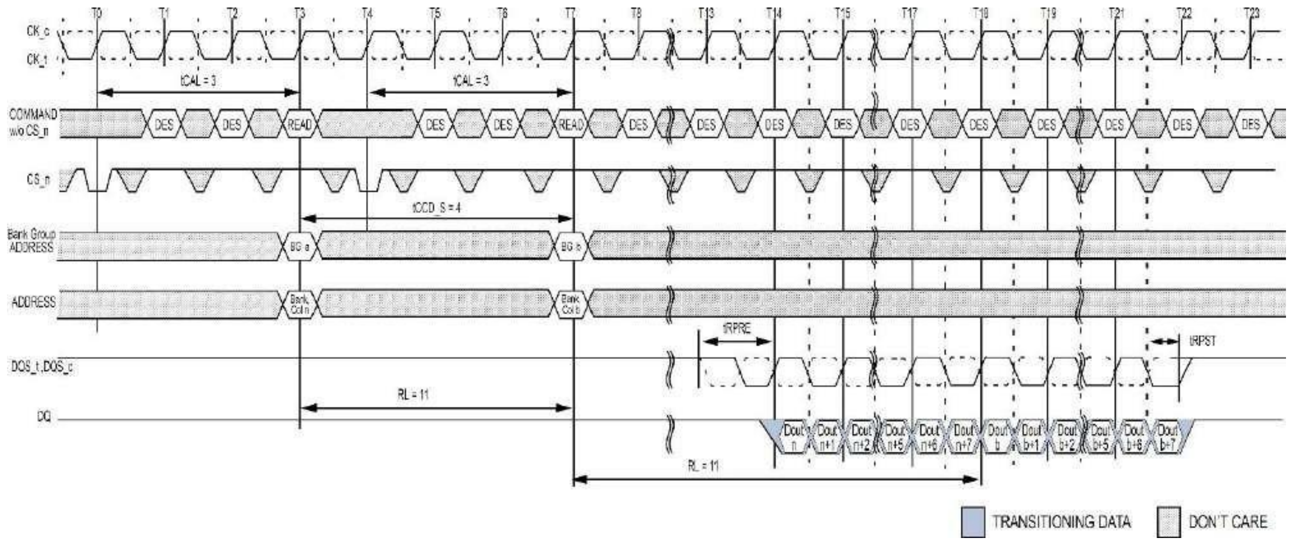
READ (BC4:Fixed) to WRITE (BC4:Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE :
1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

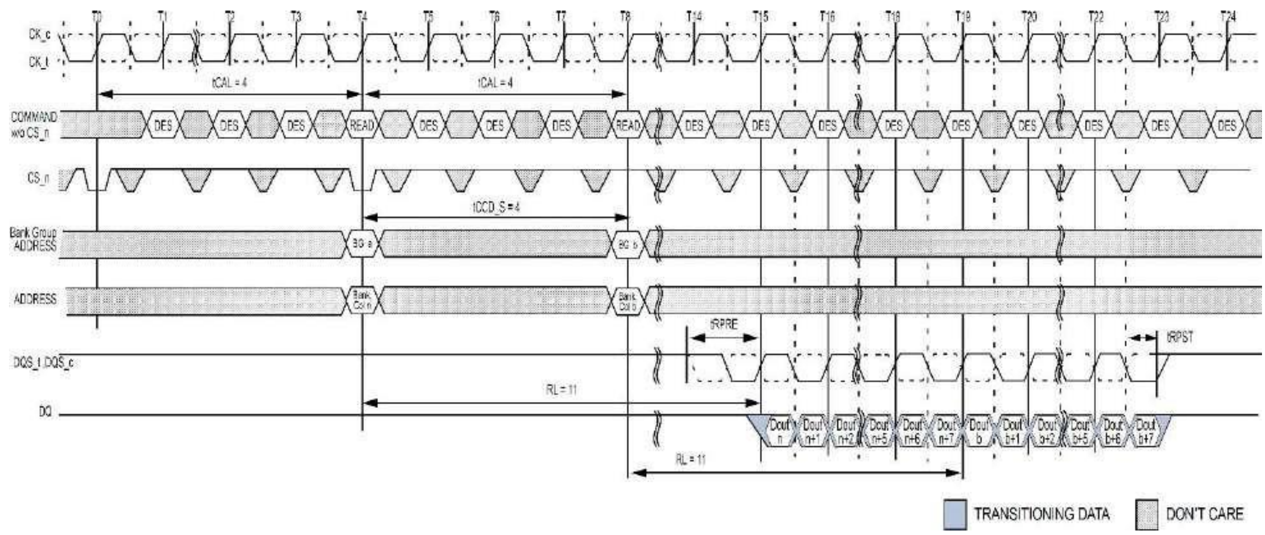
Read to Read with CS to CA Latency

Consecutive READ (BL8) with CAL(3) and 1tCK Preamble in Different Bank Group



NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T3 and T7.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Consecutive READ (BL8) with CAL(4) and 1tCK Preamble in Different Bank Group

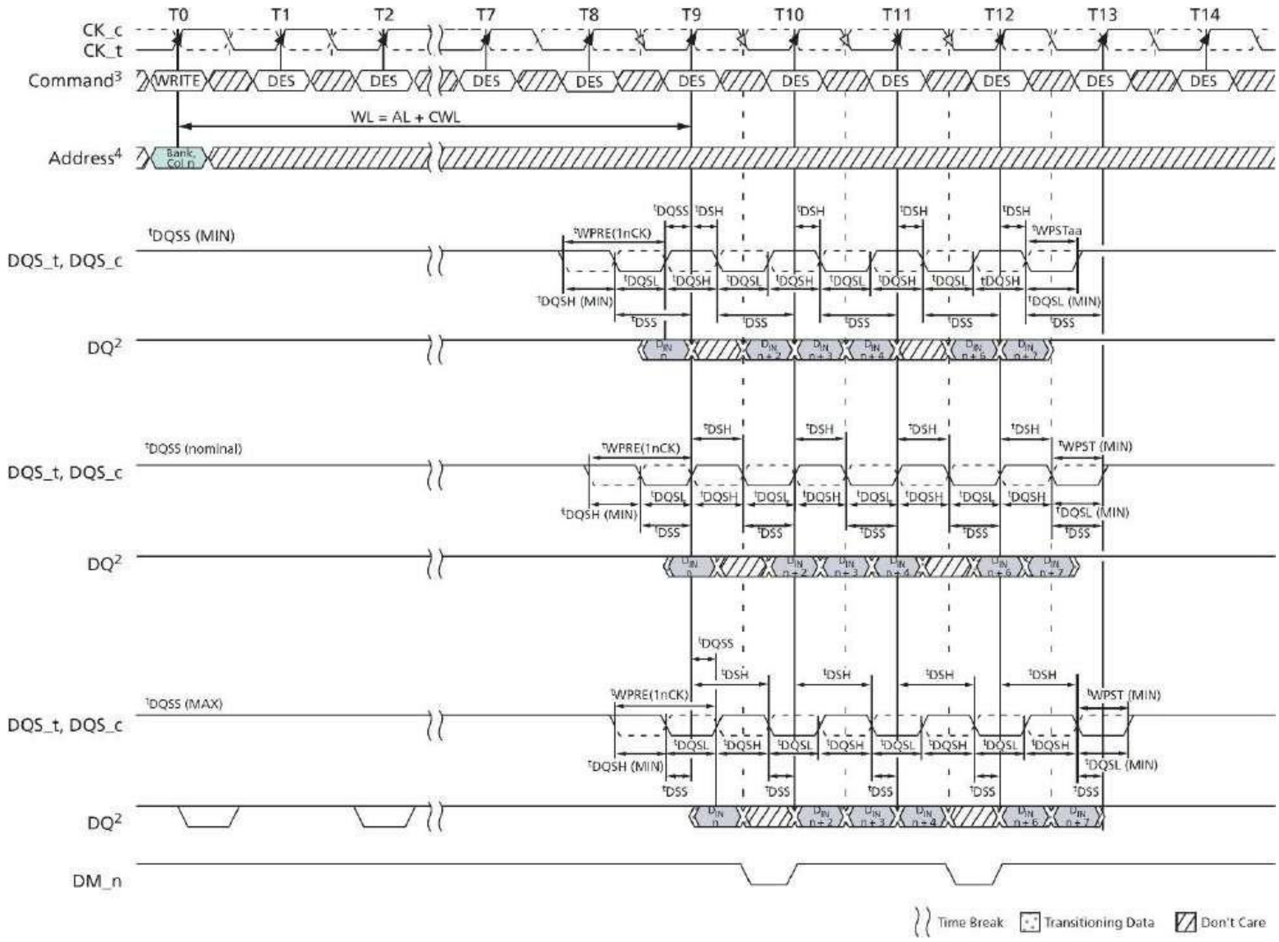


NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 4, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/address bus as when CAL is disabled.

Write Operation

Write Timing Definitions

The write timings shown in the following figures are applicable in normal operation mode, that is, when the DLL is enabled and locked.

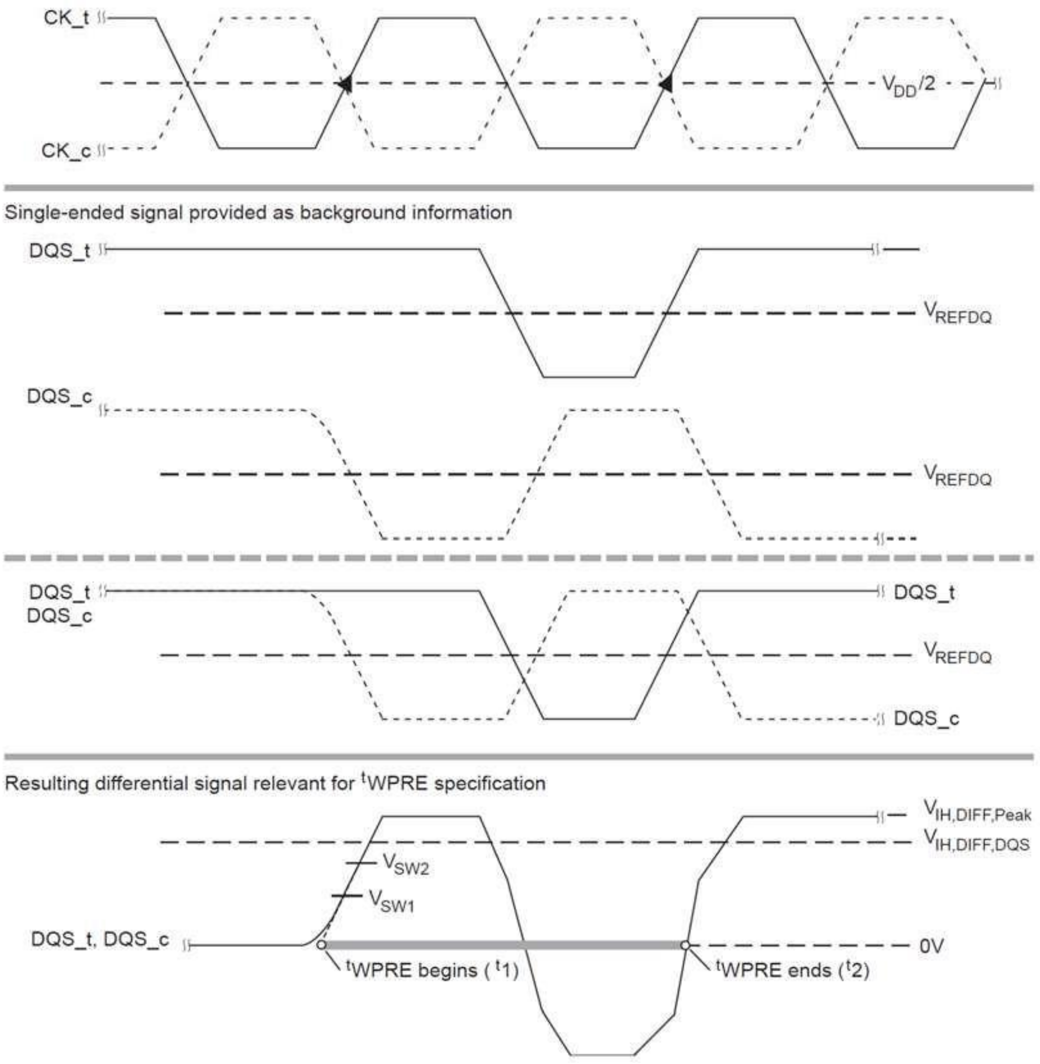


NOTE

1. BL8, WL = 9 (AL = 0, CWL = 9).
2. DIN*n* = data-in from column *n*.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during WRITE command at T0.
5. tDQSS must be met at each rising clock edge.

tWPRE Calculation

Method for calculating tWPRE transitions and endpoints

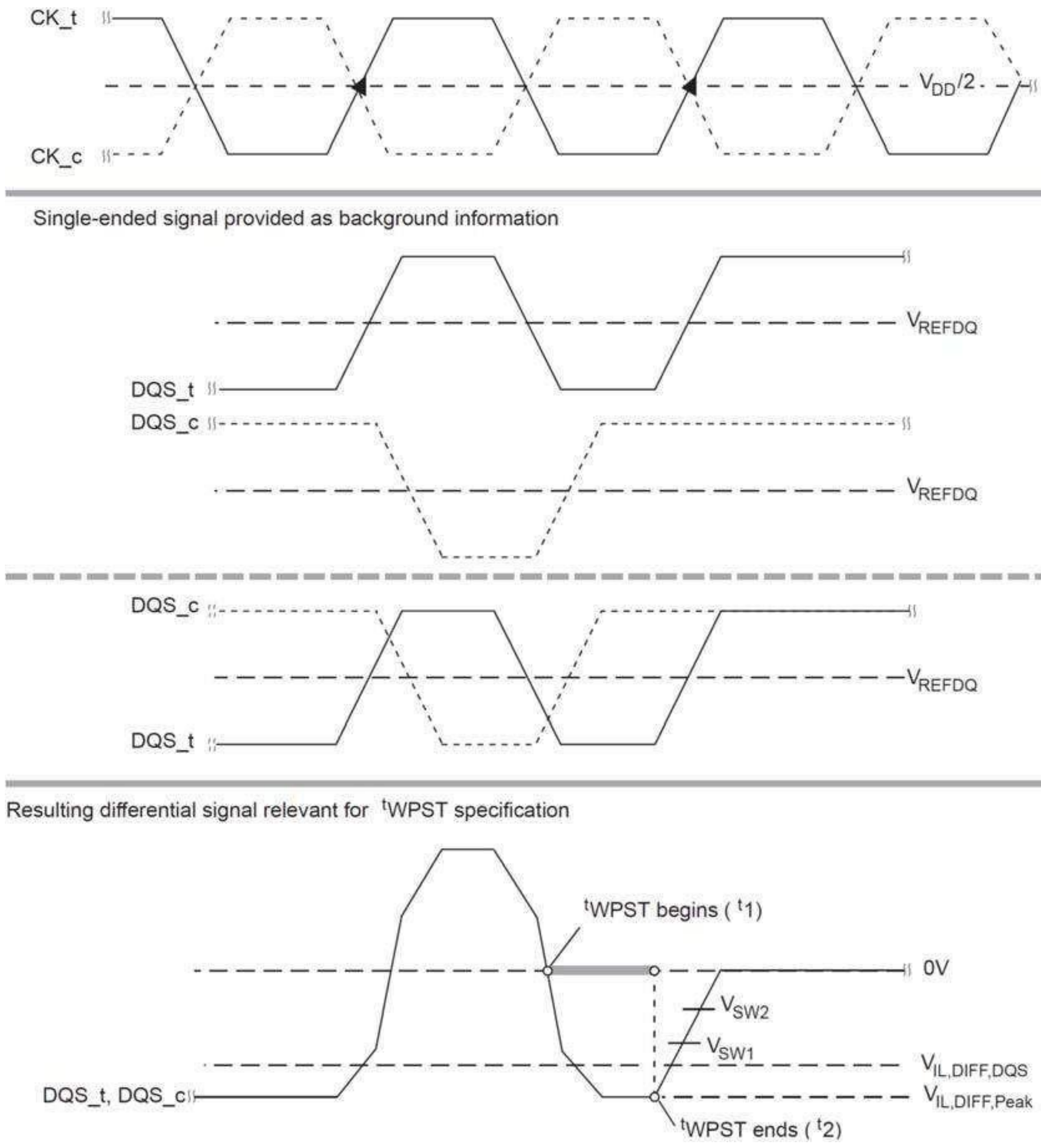


NOTE

1. Vsw1 = (0.1) × $VIH_{,diff,DQS}$.
2. Vsw2 = (0.9) × $VIH_{,diff,DQS}$.

tWPST Calculation

Method for calculating tWPST transitions and endpoints



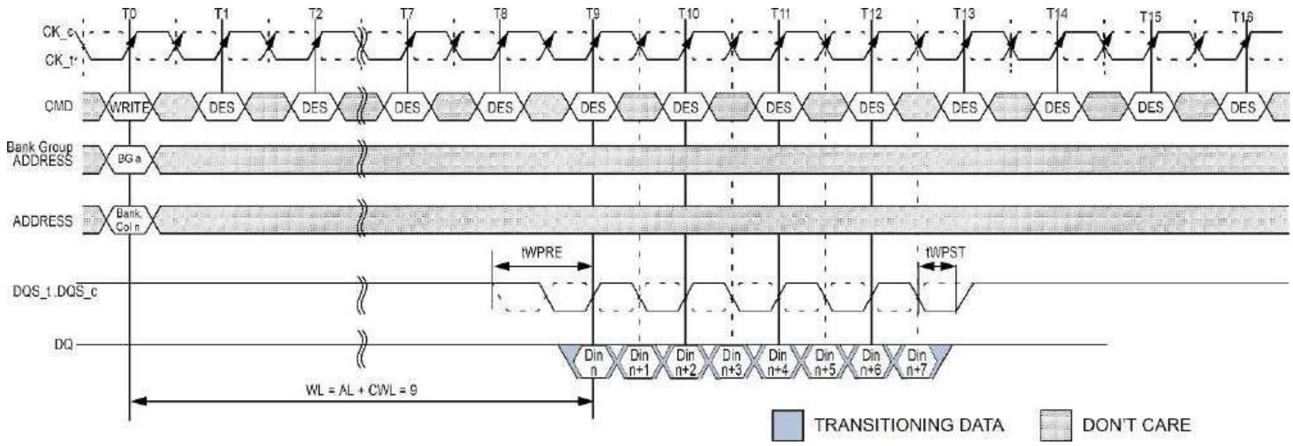
NOTE

1. Vsw1 =(0.9) × $VIL_{,diff,DQS}$.
2. Vsw2 = (0.1) × $VIL_{,diff,DQS}$.

WRITE Burst Operation

The following write timing diagrams are to help understanding of each write parameter'smeaning and are just examples. The details of the definition of each parameter will be defined separately. In these write timing diagram, CK and DQS are shown alignedand also DQS and DQ are shown center aligned for illustration purpose.

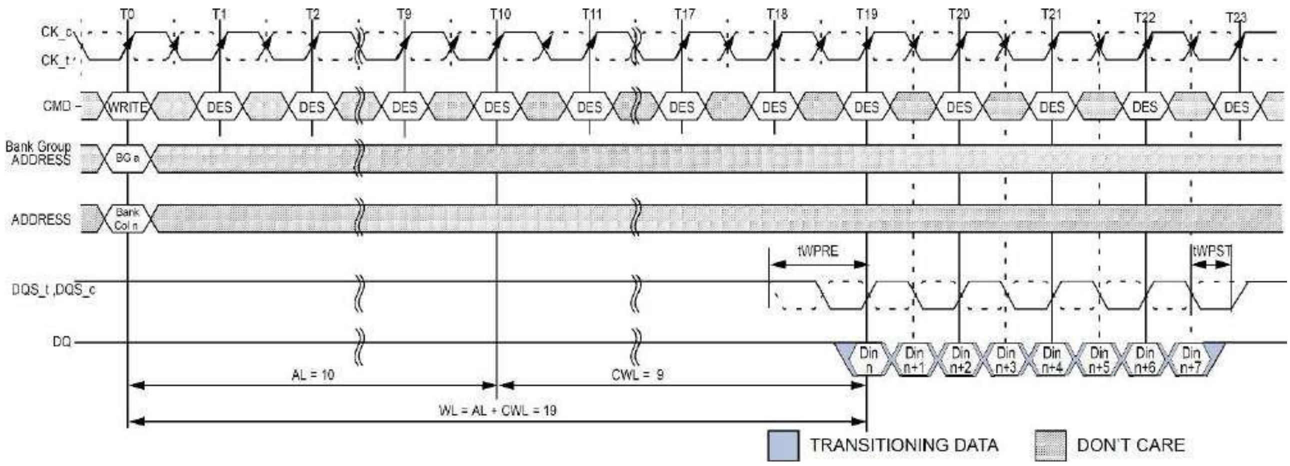
WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)



NOTE :

1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

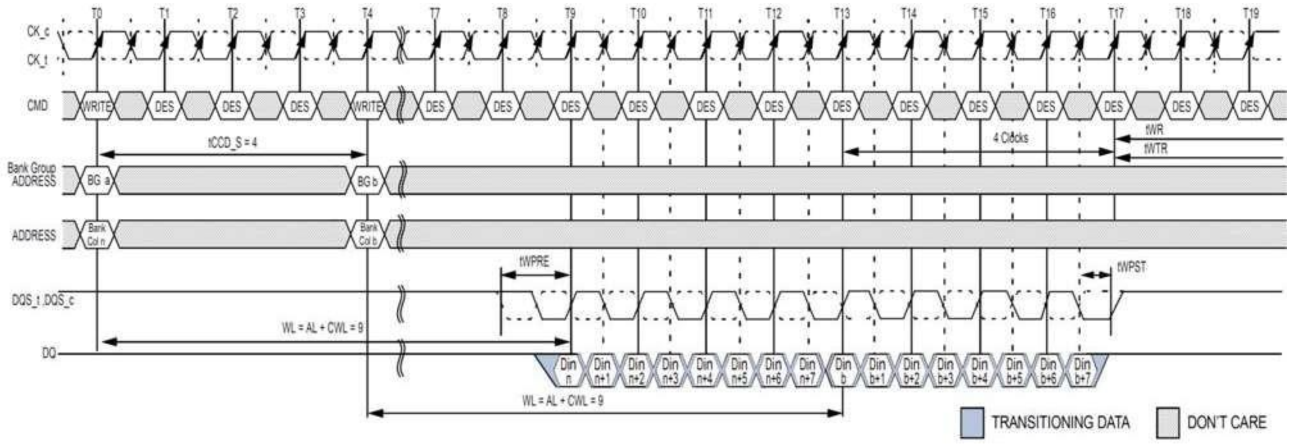
WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)



NOTE :

1. BL = 8 ,WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

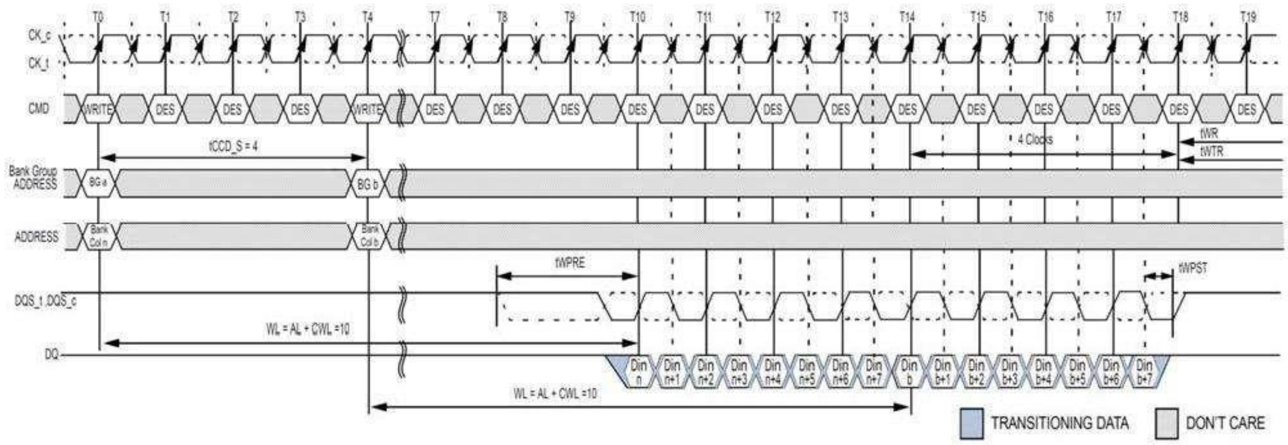
Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE :

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

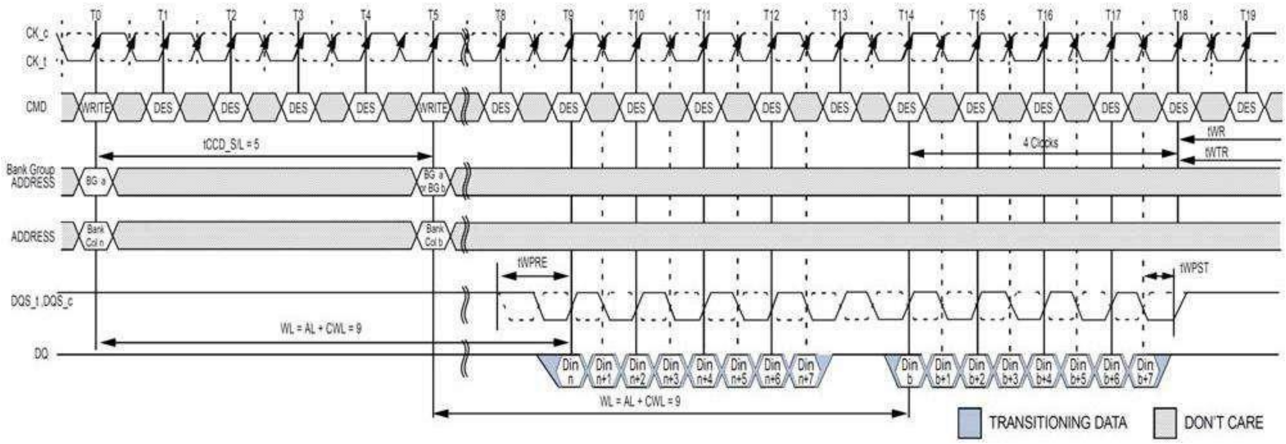
Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE :

1. BL = 8 ,AL = 0, CWL = 9 + 1 = 107, Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time(tWR) and write timing parameter(tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

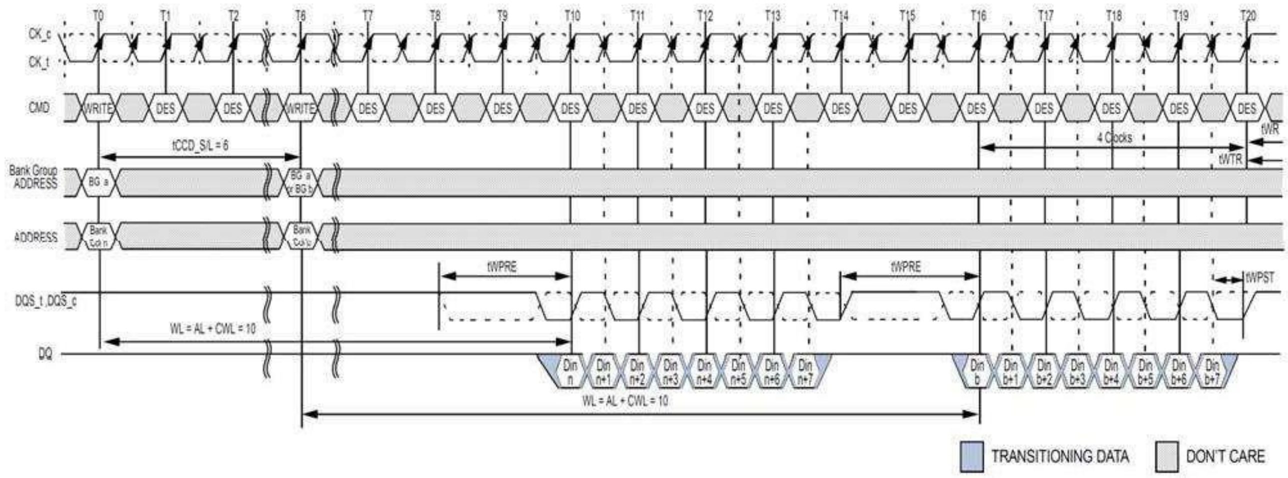
Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE:

1. BL = 8 ,AL = 0, CWL = 9 , Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

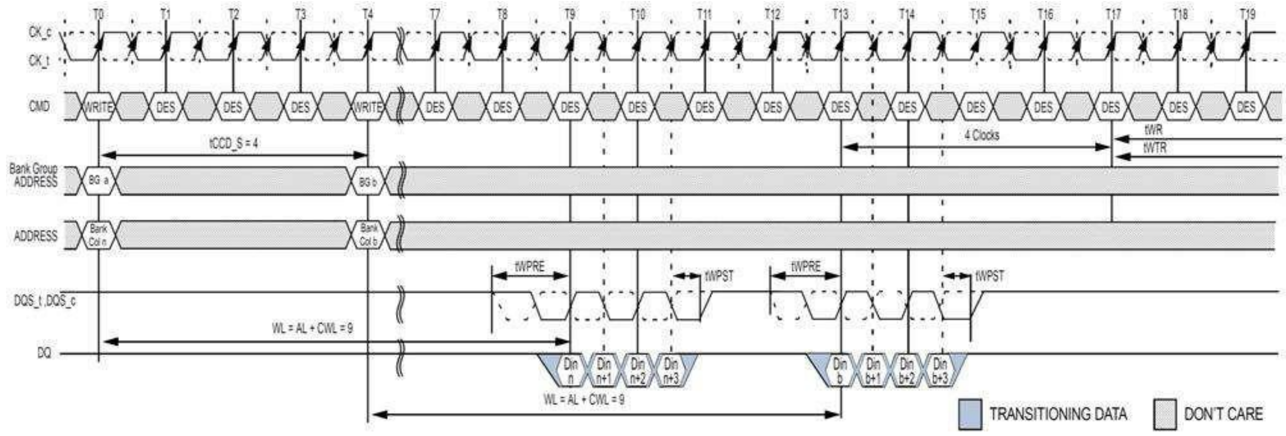
Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE:

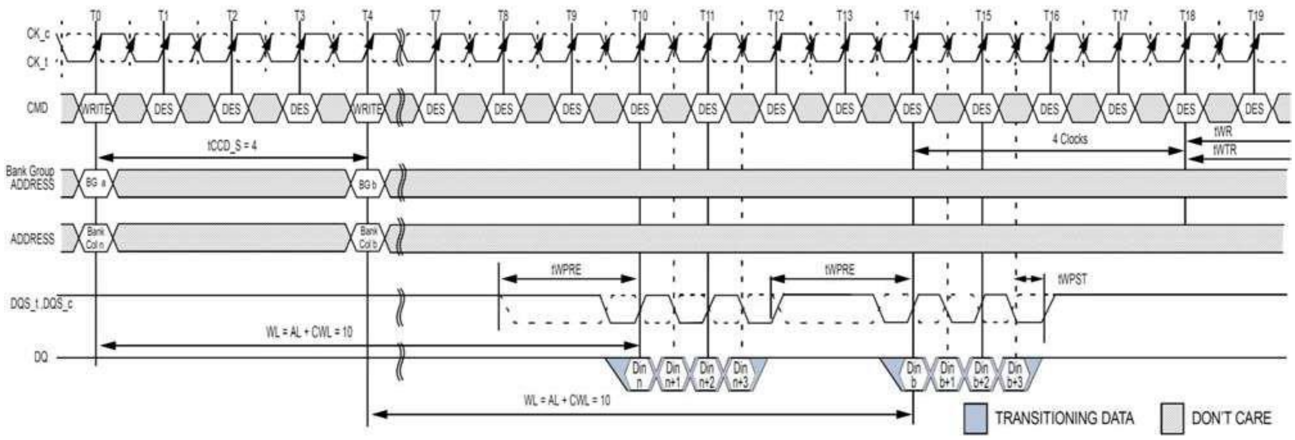
1. BL = 8 ,AL = 0, CWL = 9 + 1 = 108 , Preamble = 2tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. tCCD_S/L=5 isn't allowed in 2tCK preamble mode.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



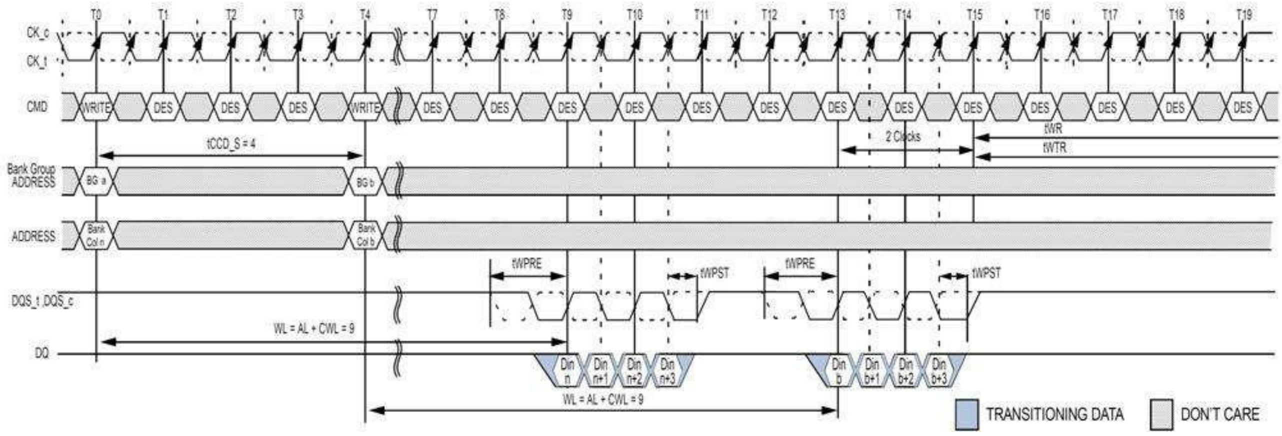
NOTE:
1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group



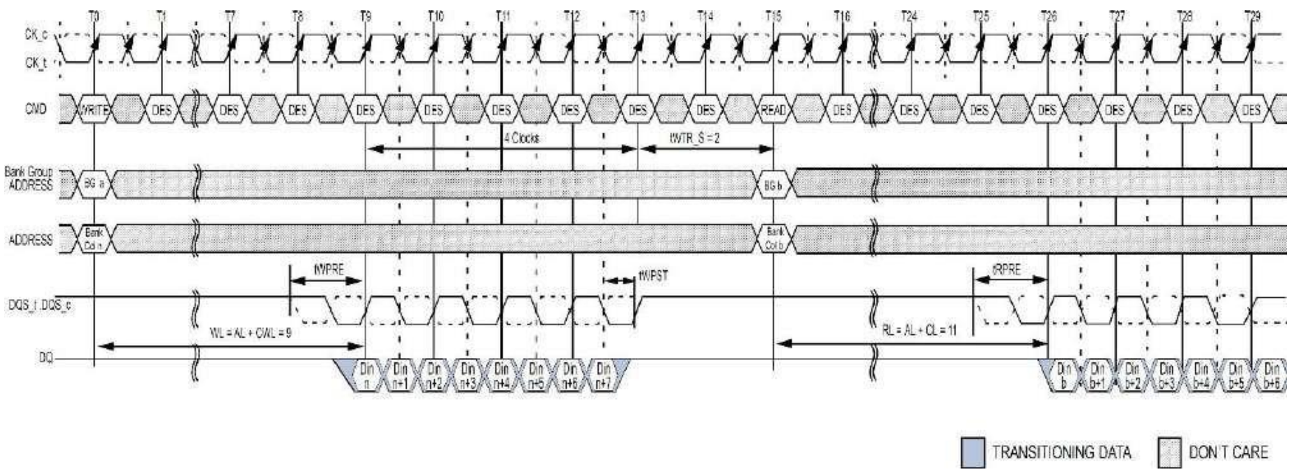
NOTE:
1. BC = 4, AL = 0, CWL = 9 + 1 = 107 , Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group



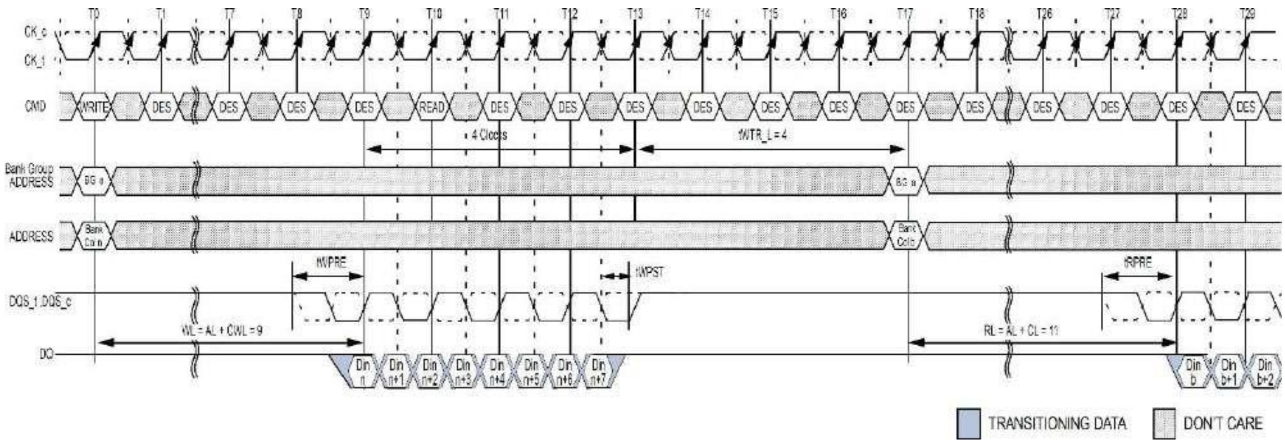
NOTE:
1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



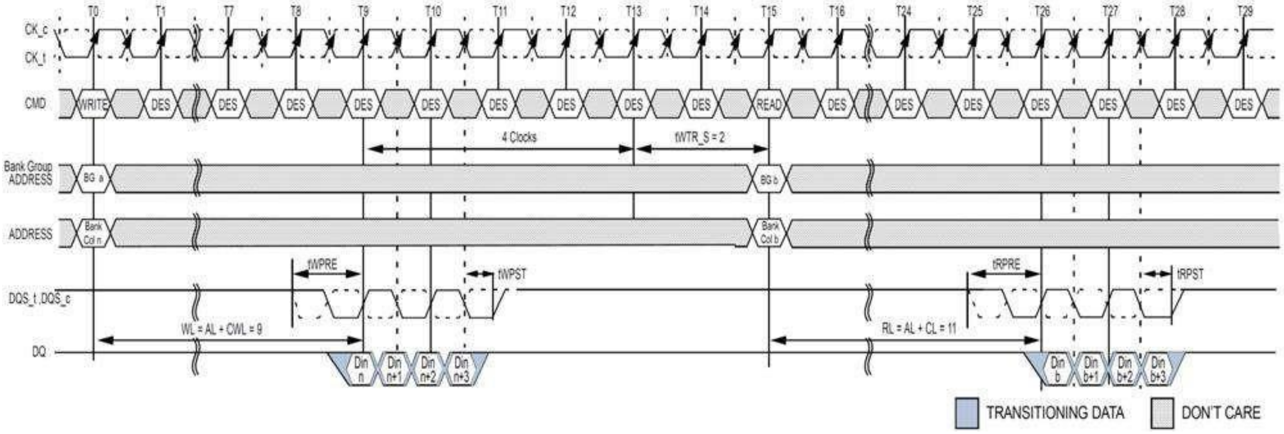
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n(or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



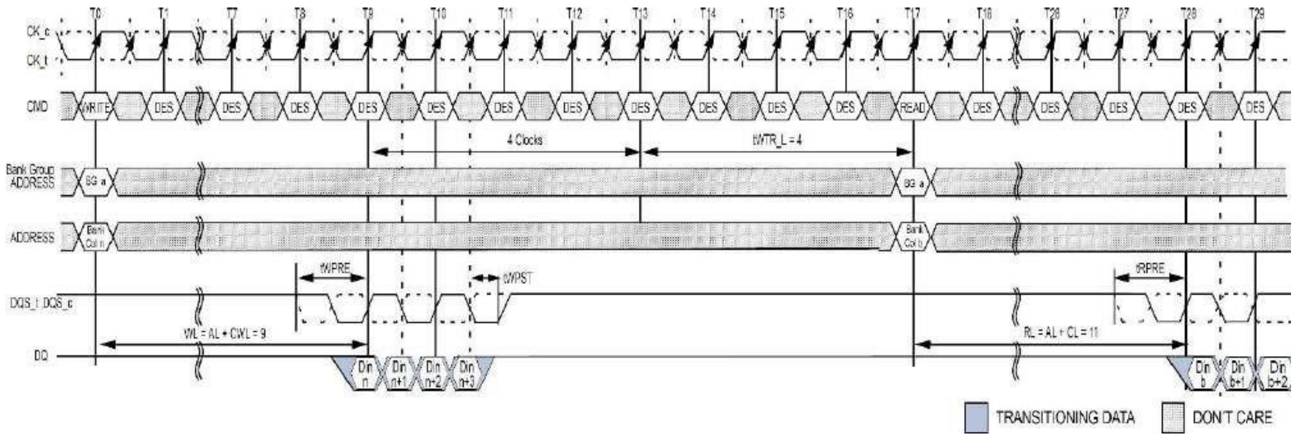
NOTE:
1. BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Different Bank Group



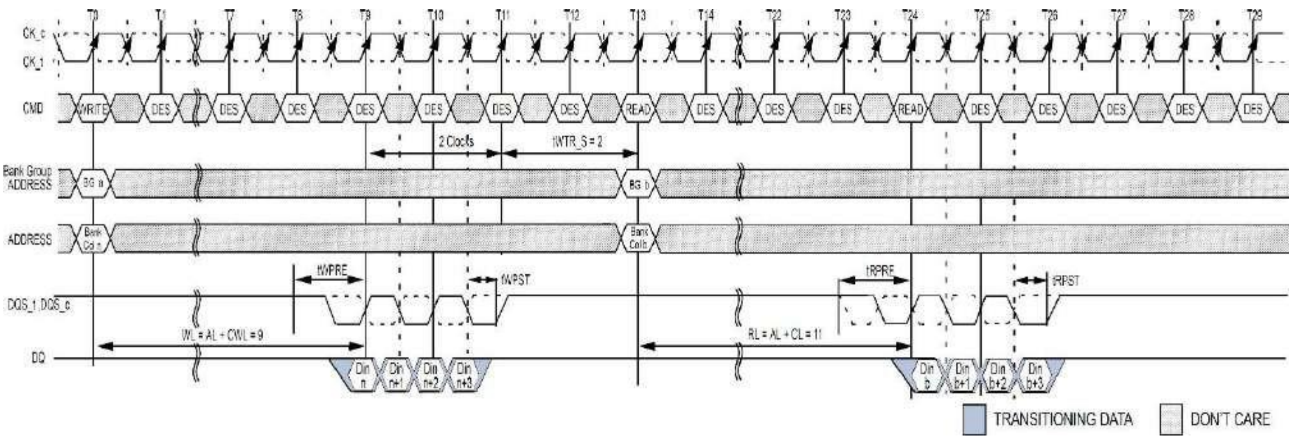
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



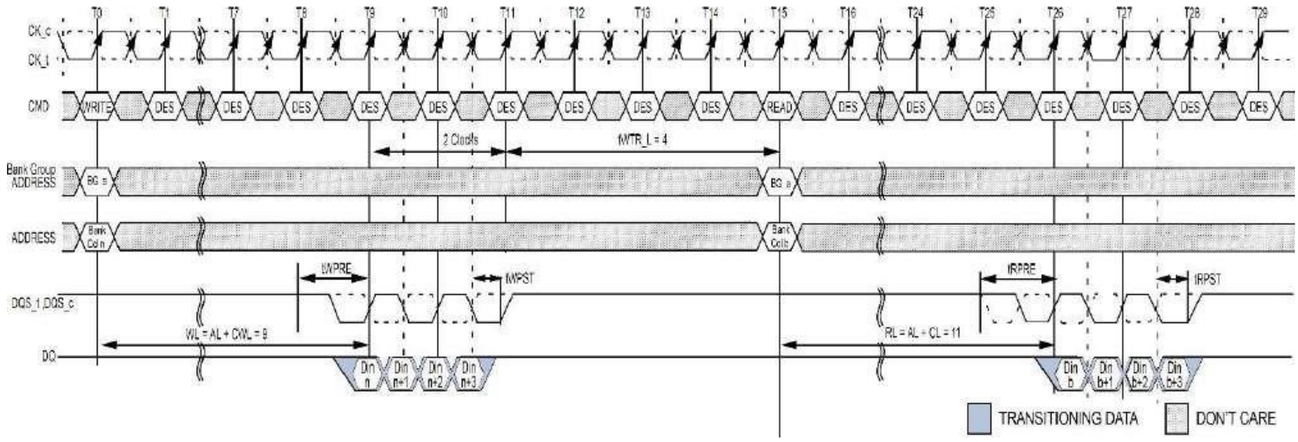
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Different Bank Group



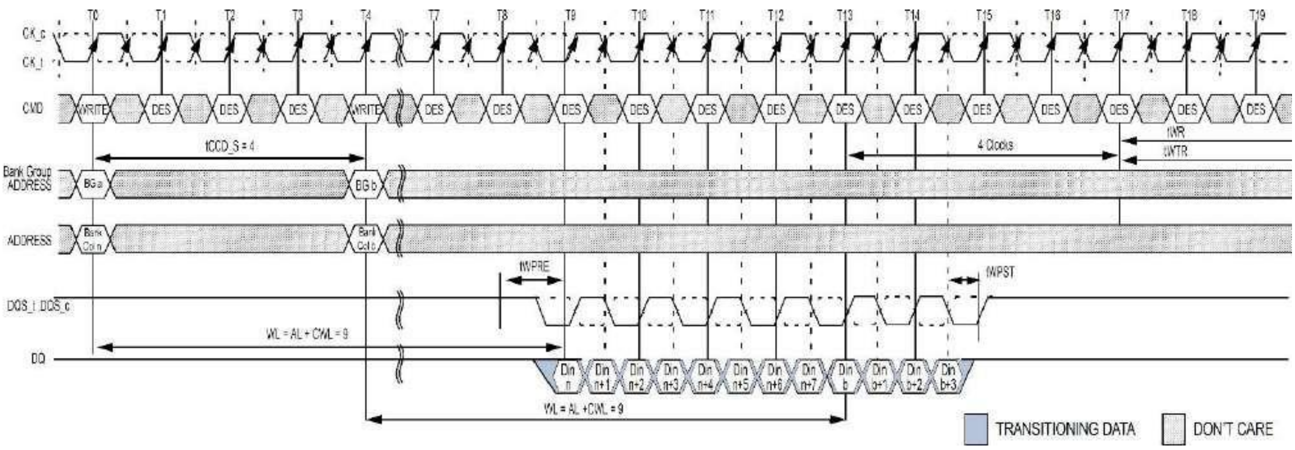
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Same Bank Group



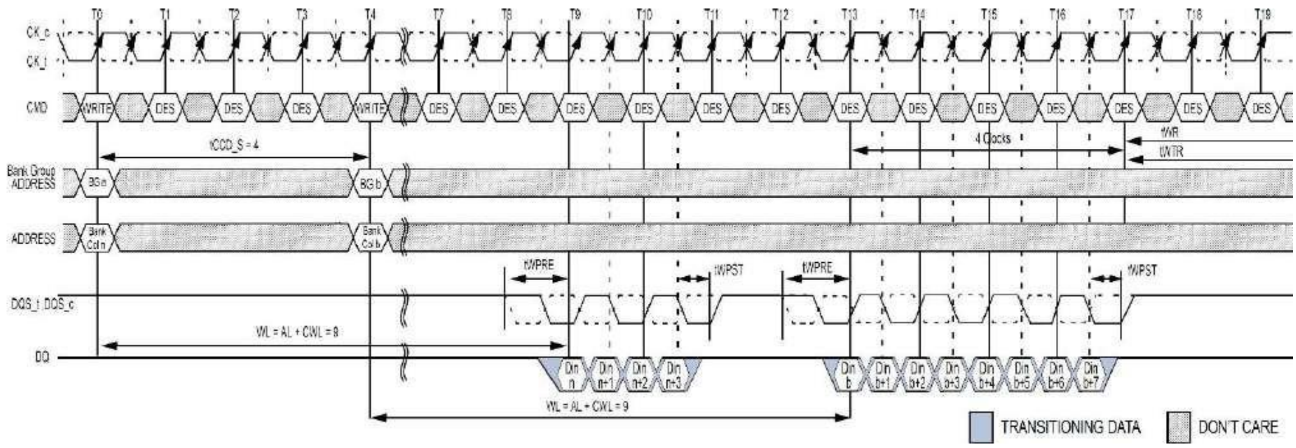
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



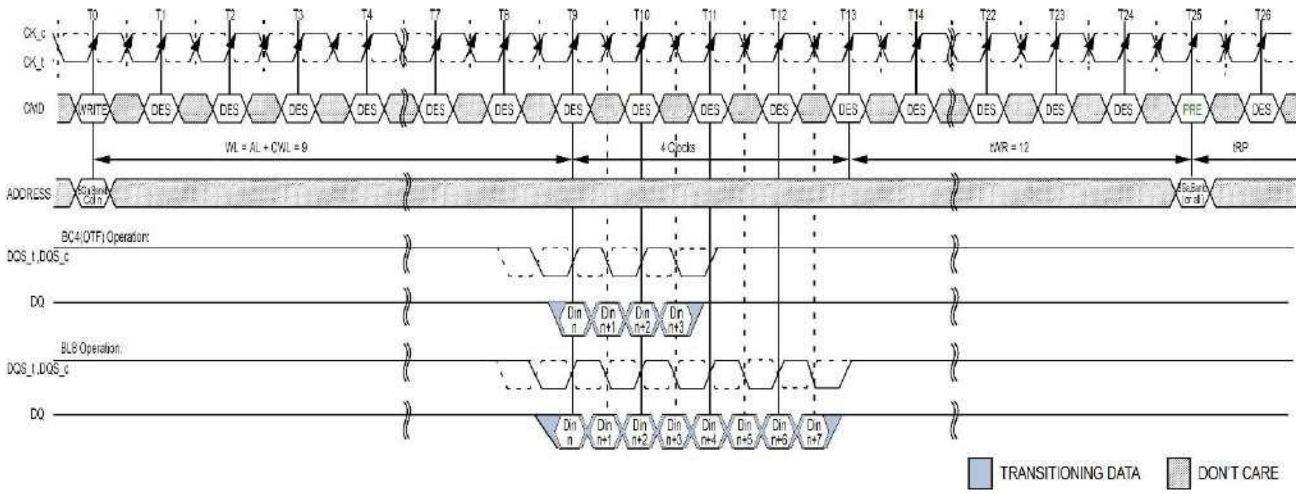
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BC4) OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



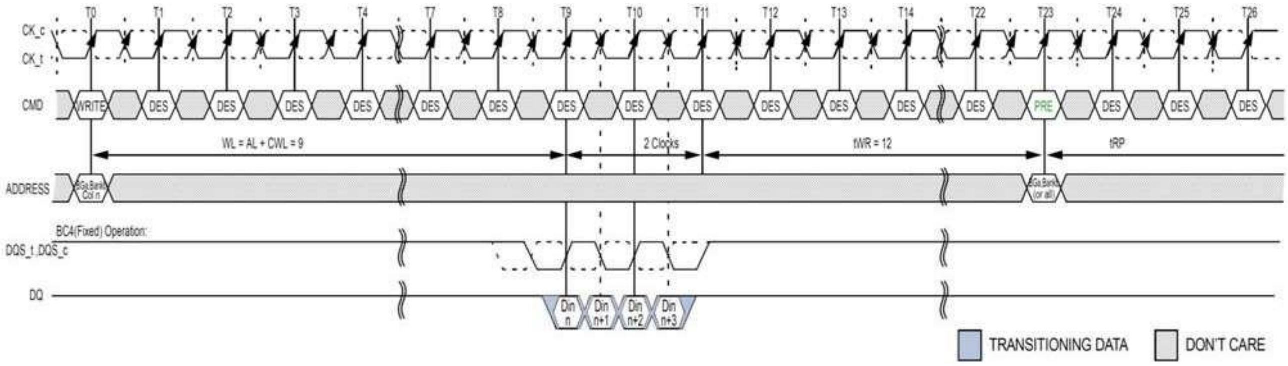
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:0] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

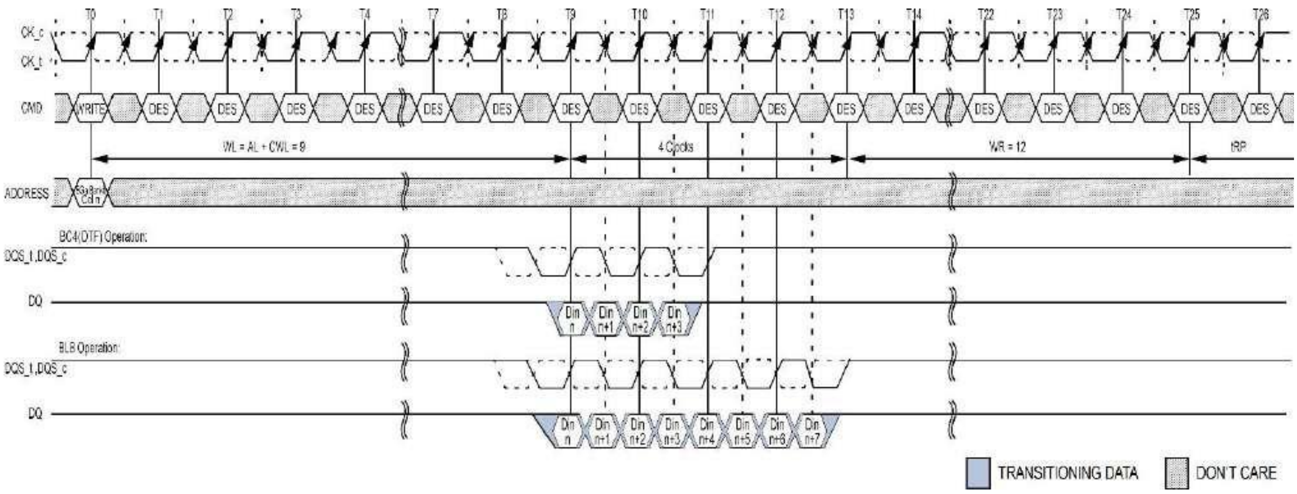
WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



NOTE:

1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

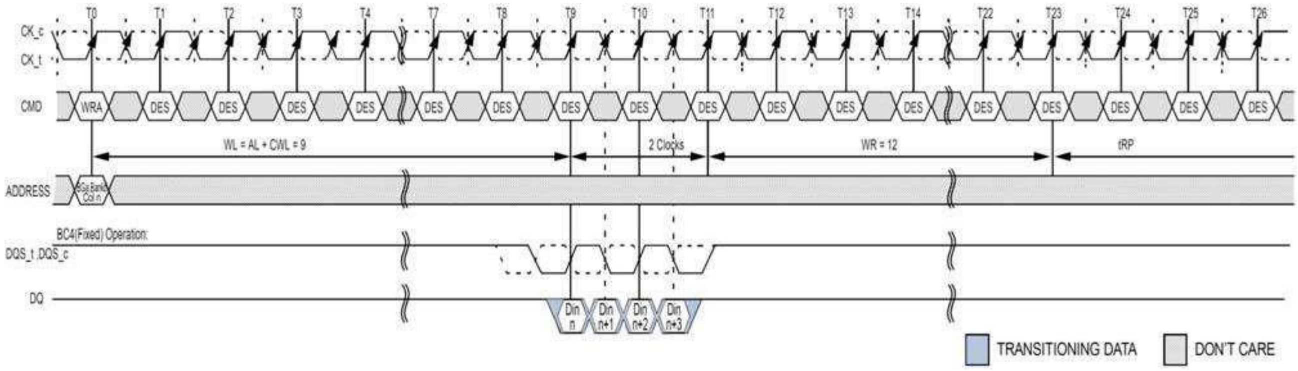
WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



NOTE:

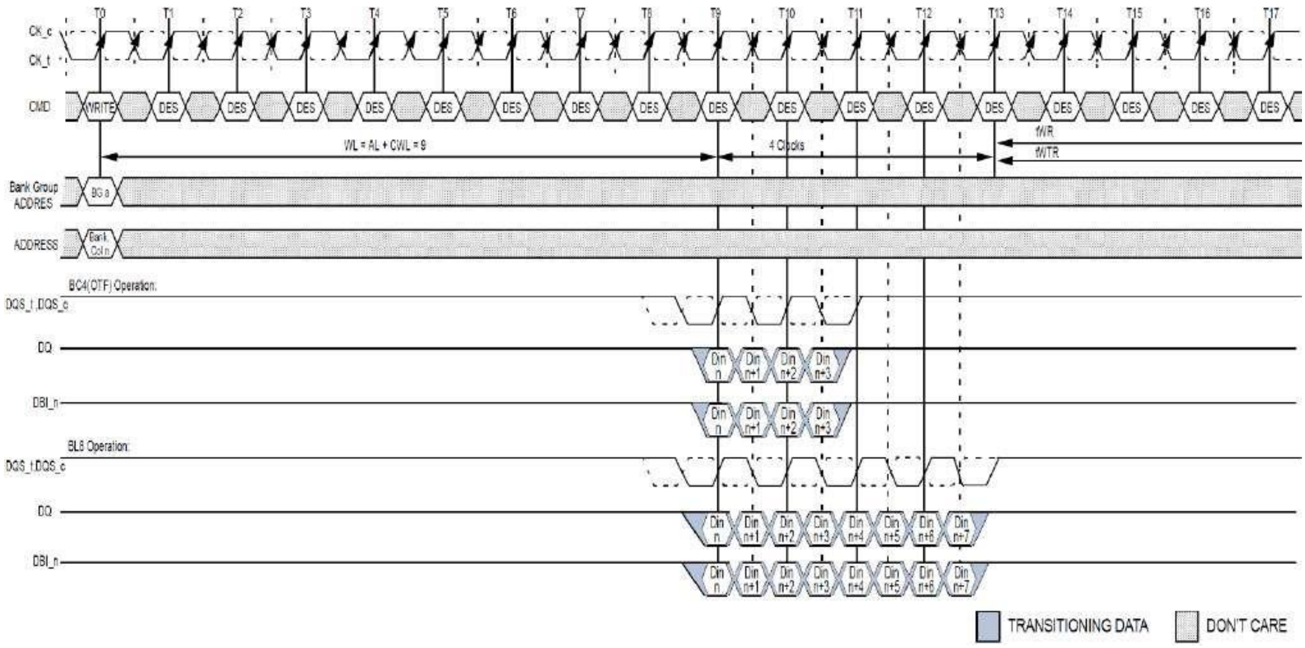
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



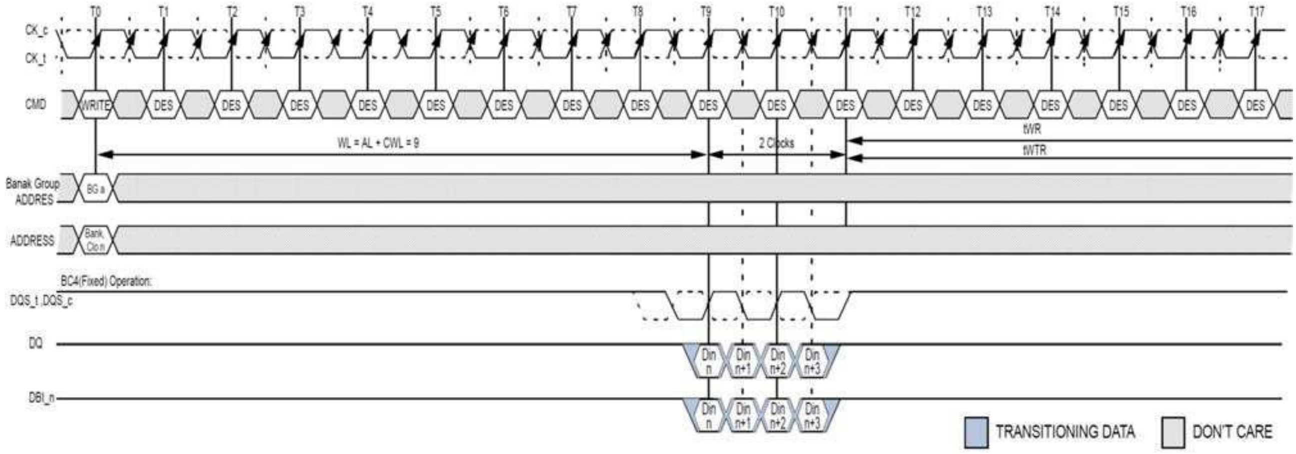
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



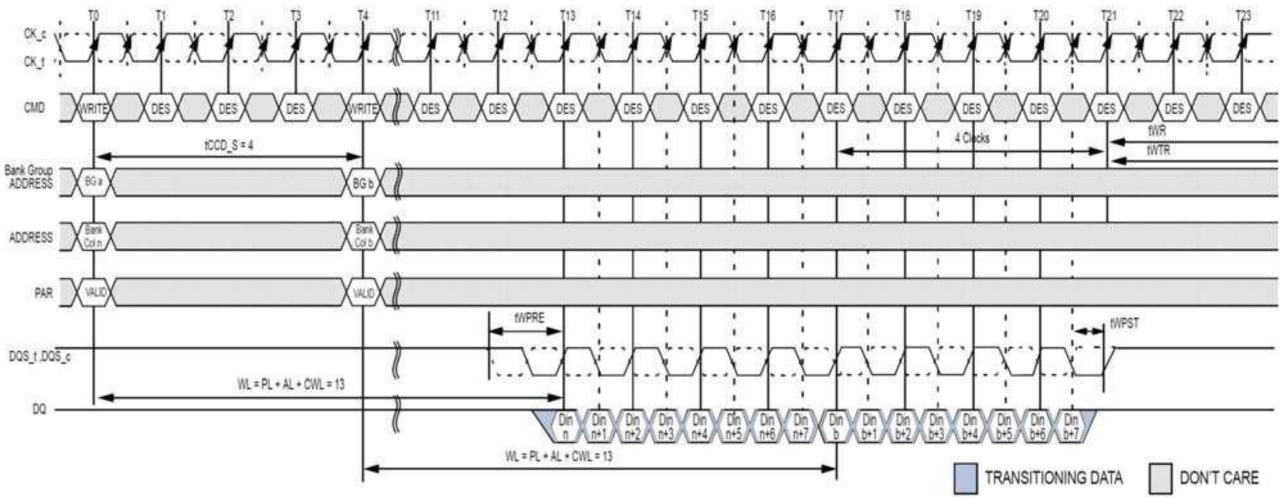
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13

WRITE (BC4) Fixed with 1tCK Preamble and DBI



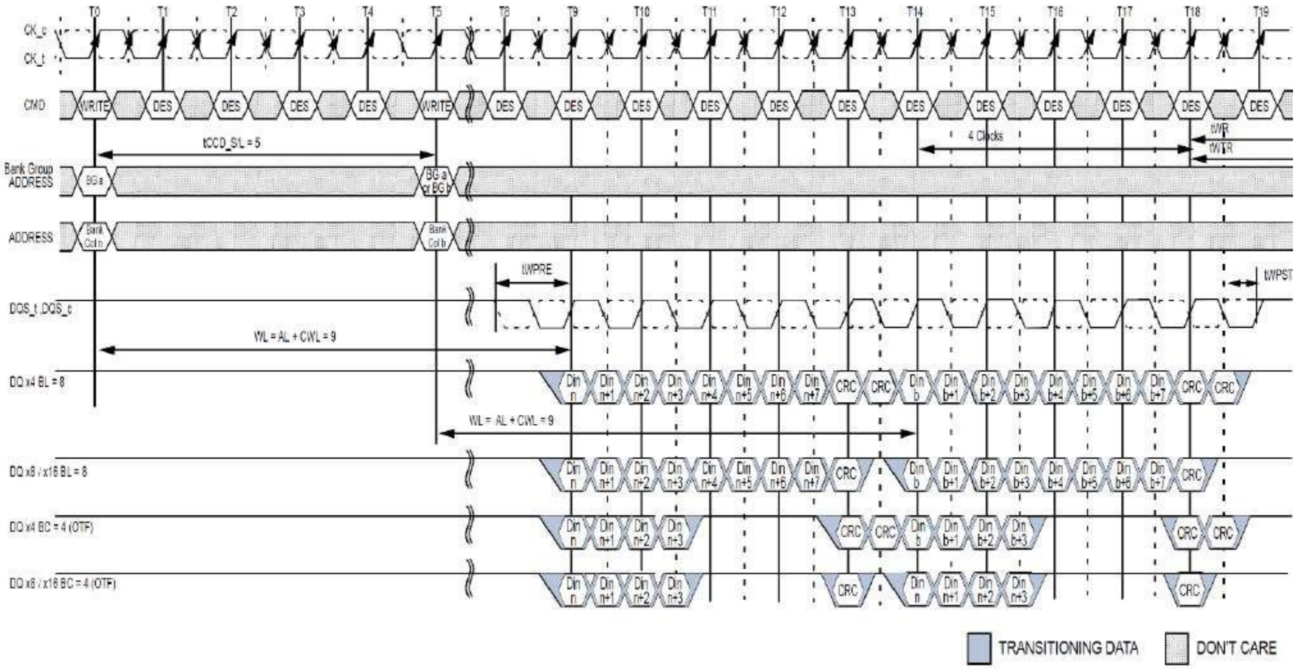
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



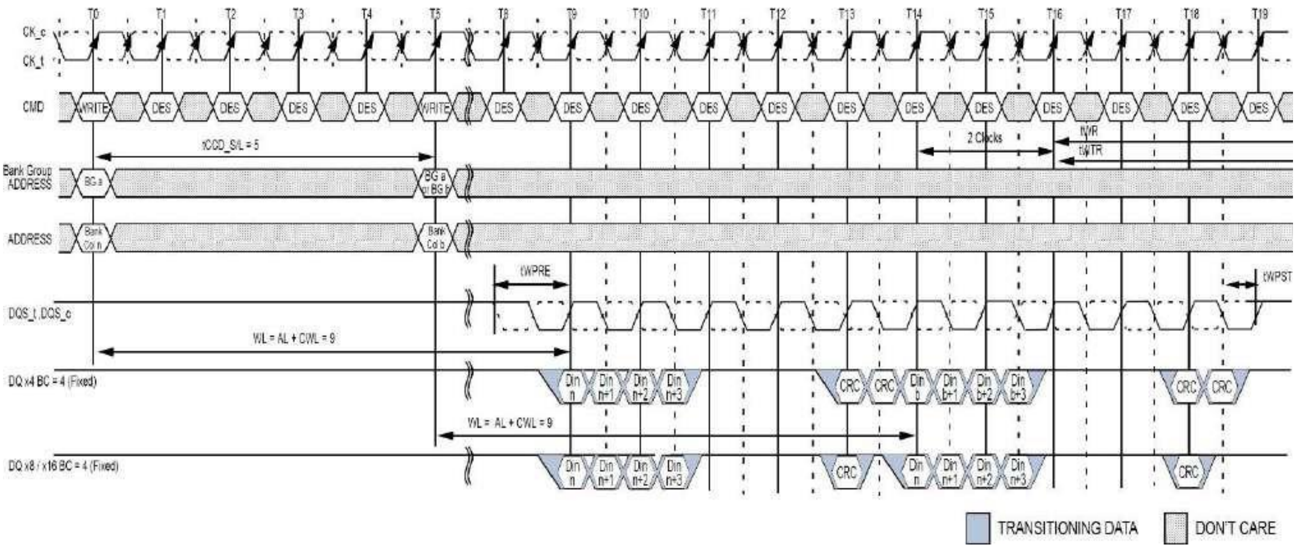
NOTE:
1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.
5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21

Consecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



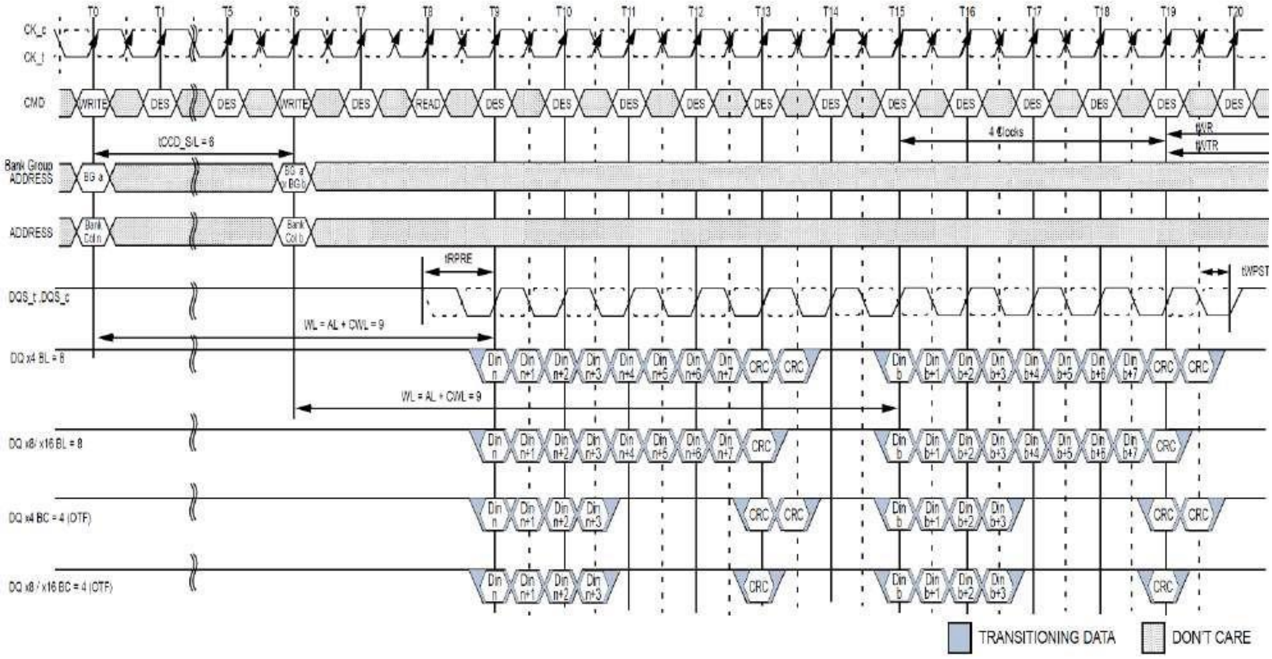
NOTE:
1. BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.
5. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

Consecutive WRITE (BC4)Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



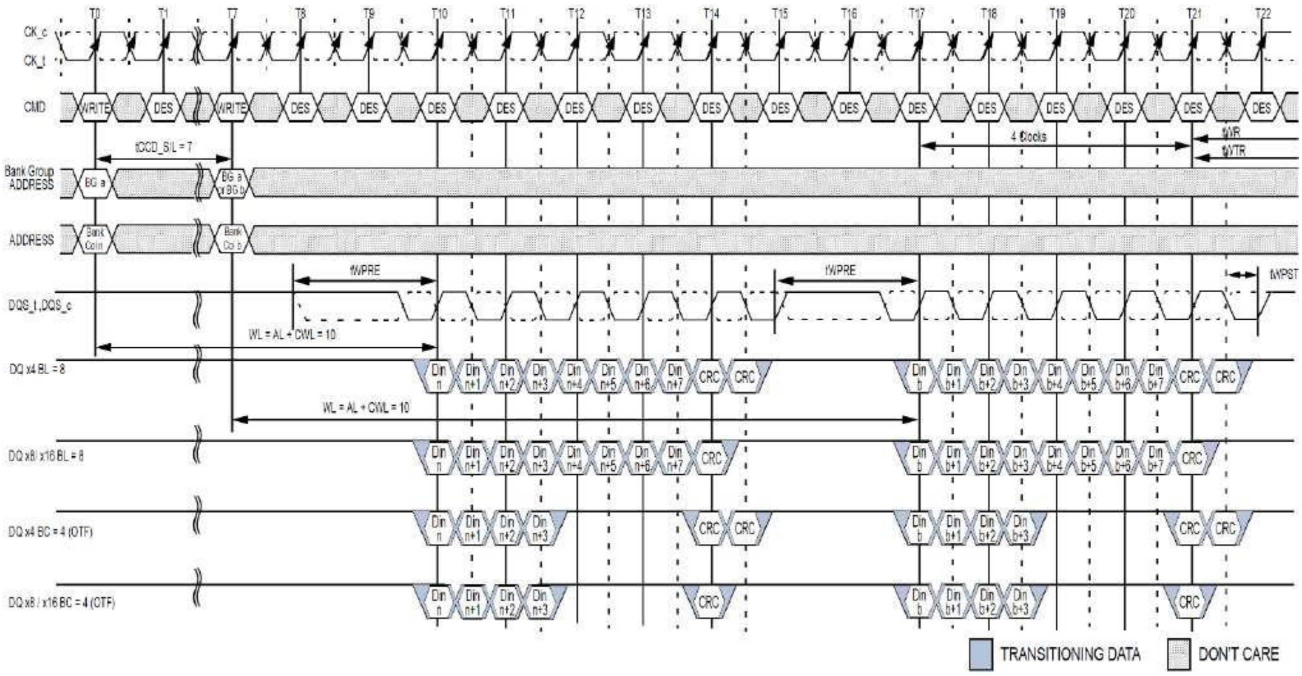
NOTE:
1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, CRC = Enable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

Nonconsecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:
1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 =1 during WRITE command at T0 and T6.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T6.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

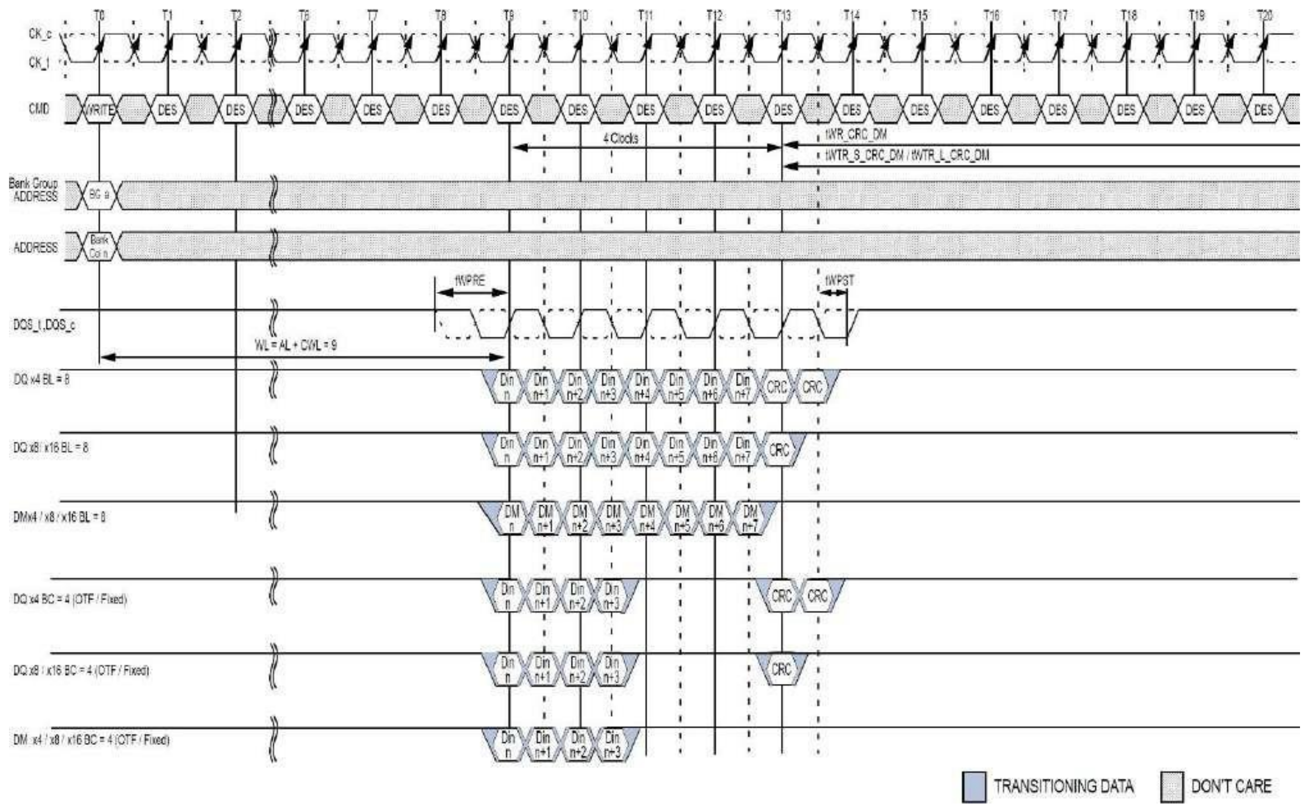
Nonconsecutive WRITE (BL8/BC4)OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8, AL = 0, CWL = 9 + 1 = 109, Preamble = 2tCK, tCCD_S/L = 7
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T7.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T7.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group



NOTE:

1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

Refresh Command

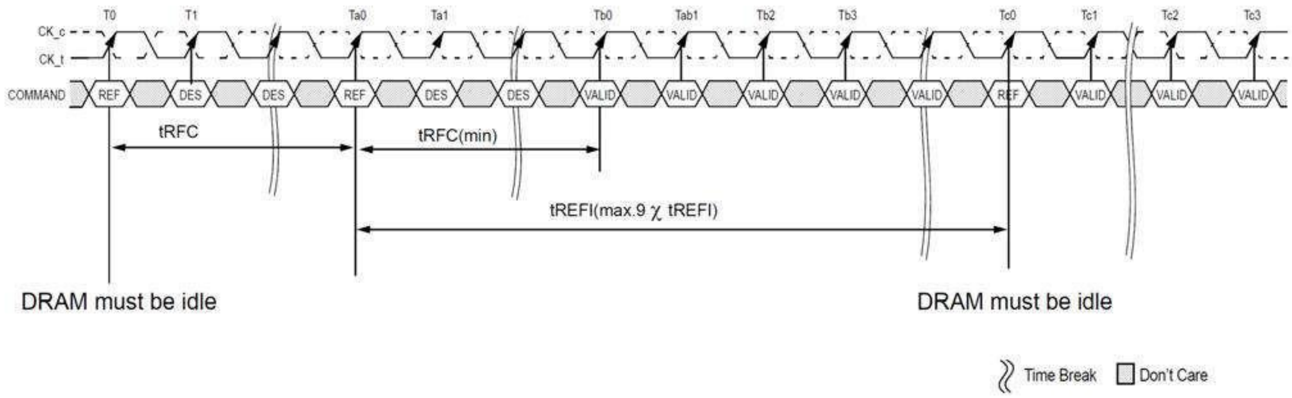
The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS_n, RAS_n/A16 and CAS_n/A15 are held Low and WE_n/A14 and ACT_n are held High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure X. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when DRAM is in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be postponed respectively during operation of the DDR4 SDRAM, meaning that at no point in time more than a total of 8,16,32 Refresh commands are allowed to be postponed for 1X,2X,4X Refresh mode respectively.

When 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI. In 2X and 4X Refresh mode, it’s limited to 17 x tREFI2 and 33 x tREFI4. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be pulled in respectively, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8/16/32, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI , 17 x tRFEI2 and 33 x tREFI4 respectively. At any given time, a maximum of 16 REF/32REF 2/64REF 4 commands can be issued within 2 x tREFI/ 4 x tREFI2/ 8 x tREFI4.

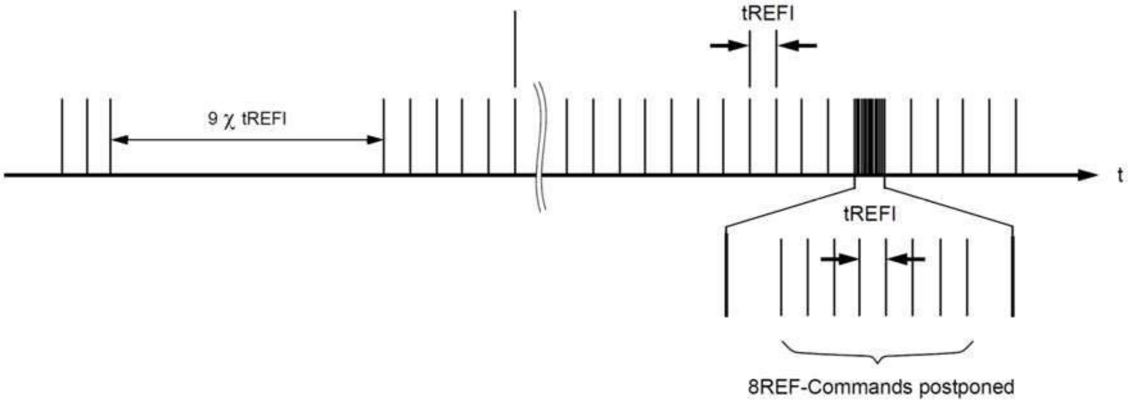
Refresh Command Timing (Example of 1x Refresh mode)

NOTE :

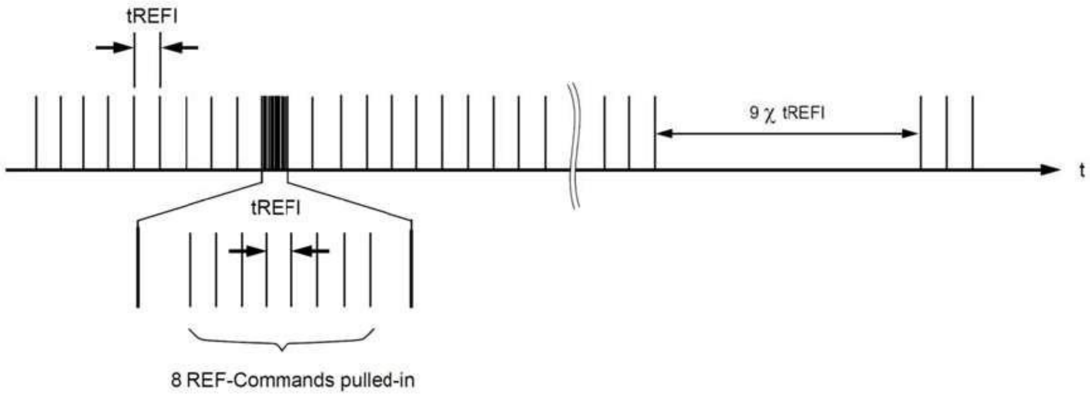


1. Only DES commands allowed after Refresh command registered untill tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Postponing Refresh Commands (Example of 1X Refresh mode)



Pulling-in Refresh Commands (Example of 1X Refresh mode)



Self refresh Operation

The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. .DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and RTT_PARK set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK asynchronously during tXSDLL when RTT_PARK is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self- Refresh.

When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VREFCA) must be at valid levels. DRAM internal VREFDQ generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VREFDQ circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VREFDQ generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

1. Commands that do not require locked DLL:
   - tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, tXSFast - ZQCL, ZQCS, MRS commands.
   - For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.

Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

2. Commands that require locked DLL:
   - tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8

Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in "ZQ Calibration Commands" on Section 4.12. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR4 SDRAM can be put back into Self-Refresh mode or Power down mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. Low level of ODT pin must be registered on each positive clock edge during tXSDLL when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

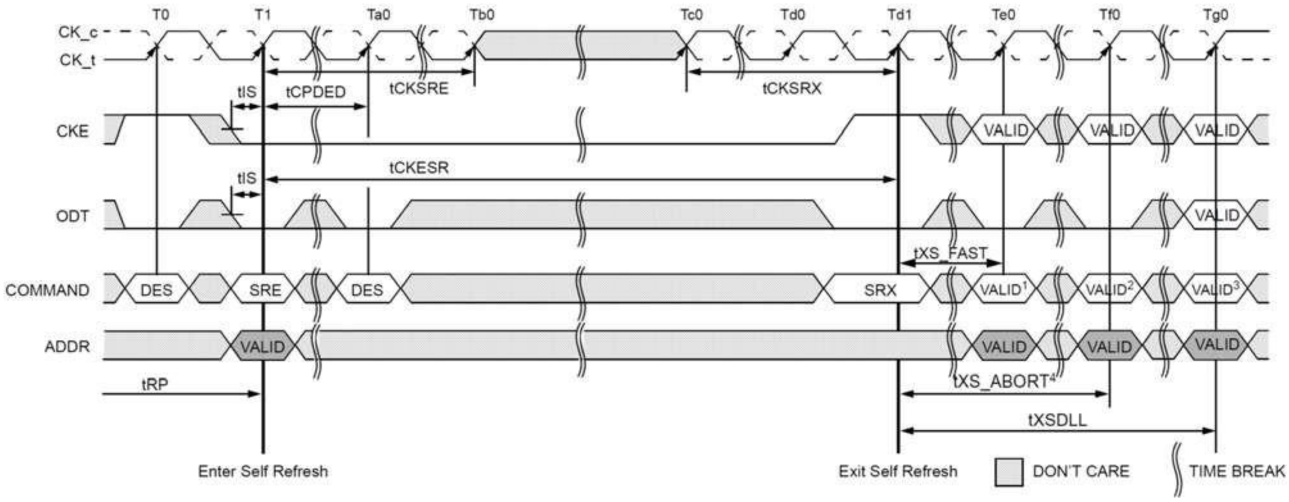
The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.

The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.

A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses tXS timings.

If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

Self-Refresh Entry/Exit Timing



NOTE :

1. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.
2. Valid commands not requiring a locked DLL.
3. Valid commands requiring a locked DLL.
4. Only DES is allowed during tXS_ABORT.

Low Power Auto Self Refresh

DDR4 devices support Low Power Auto Self-Refresh (LP ASR) operation at multiple temperatures ranges.

MR2 definitions for Low Power Auto Self-Refresh mode

A6	A7	Self-Refresh Operation Mode
0	0	Manual Mode – Normal operating temperature range
0	1	Manual Mode – Extended operating temperature range
1	0	Manual Mode – Lower power mode at a reduced operating temperature range
1	1	ASR Mode – automatically switching between all modes to optimize power for any of the temperature ranges listed above

Auto Self Refresh (ASR)

DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bits A6=1 and A7=1. The DRAM will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, the DRAM will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

Manual Modes

If ASR mode is not enabled, the LP ASR Mode Register must be manually programmed to one the three self-refresh operating modes listed above. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the selfrefresh according to their system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exiting from self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk to data retention resulting in loss of data.

Self Refresh Function Table

MR2 A6	MR2 A7	Low-Power Auto Self Refresh Mode	Self Refresh Operation	Allowed Operating temp. range for Self Refresh Mode
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85°C DRAM Tcasemax is not exceeded to avoid any risk of data loss.	(0°C – 85°C)
0	1	Extended	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(0°C – 95°C)
1	0	Reduced	Variable or fixed self-refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM Tcasemax is not exceeded to avoid any risk of data loss.	(0°C – 45°C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption and data retention are optimized for any given operating temperature conditions	All of the above

Power down Mode

Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in following figures with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CKE and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide Rtt_Nom termination. Note that DRAM continues to provide Rtt_Park termination if it is enabled in DRAM mode register MR5 bit A8:A6 To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

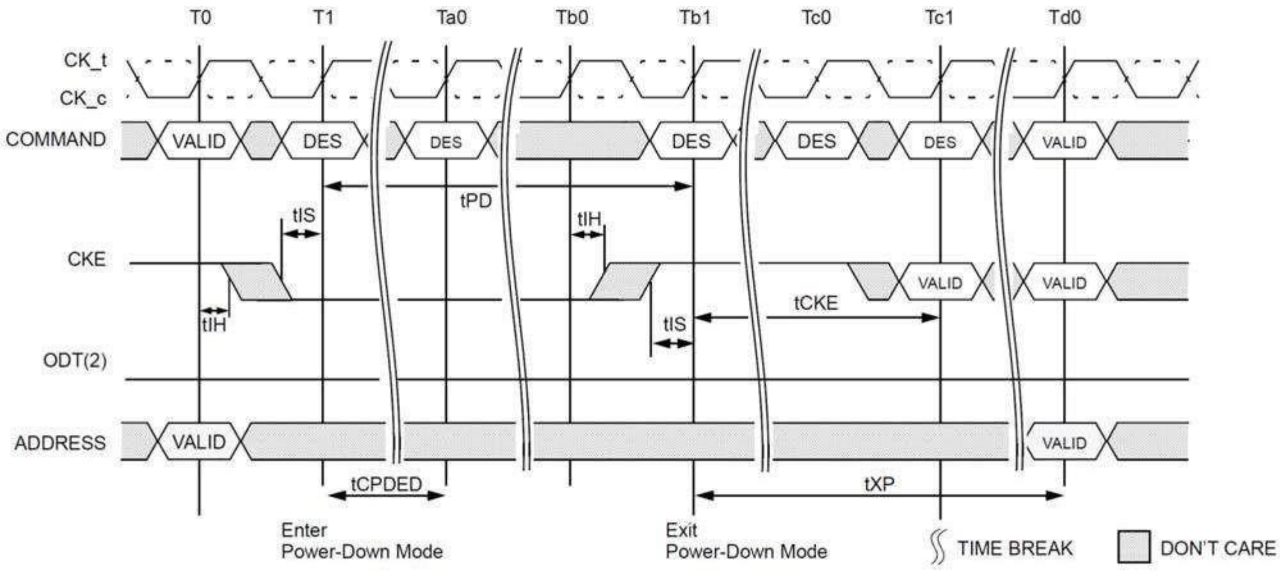
Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, RESET_n high, and a stable clock signal must be maintained at the inputs of the DDR4 SDRAM, and ODT should be in a valid state, but all other input signals are “Don’t Care.” (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until tCKE has been satisfied. DRAM ODT input signal must be at valid level when DRAM exits from power-down mode independent of MR5 bit A5 if Rtt_Nom is enabled in DRAM mode register. If DRAM Rtt_Nom is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes high. Power-down exit latency is defined in the AC specifications Table.

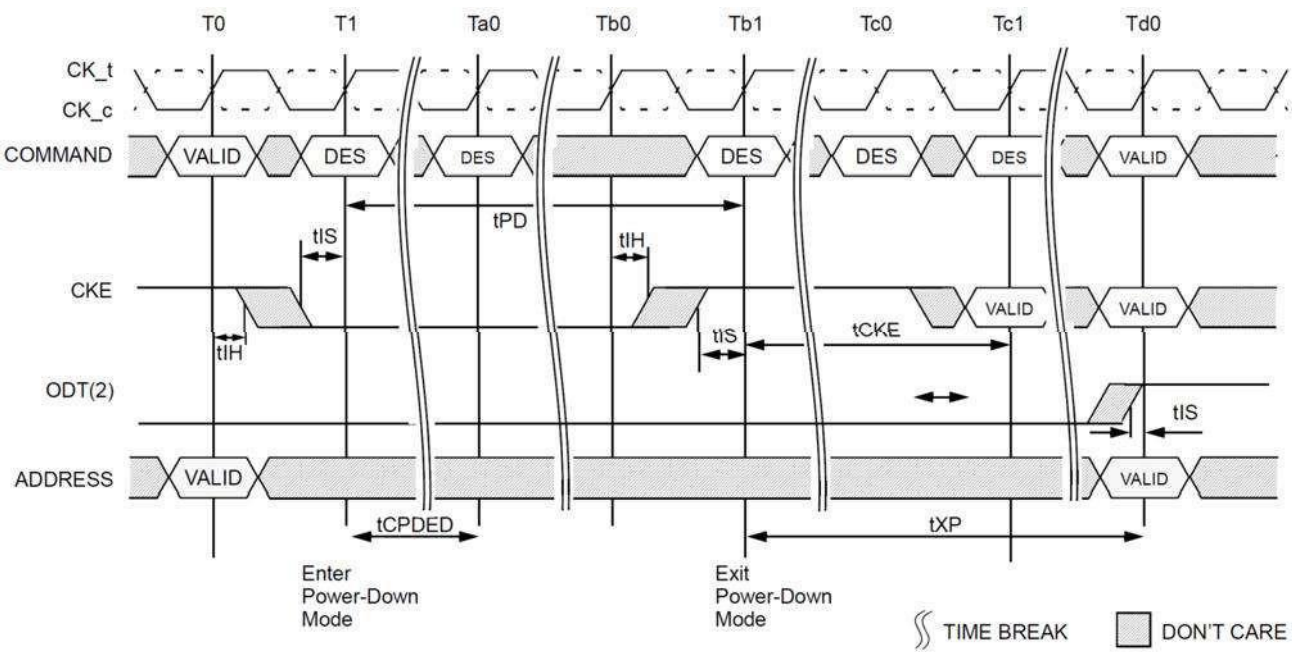
Active Power-Down Entry and Exit Timing Diagram (MR5 bit A5 =0)



NOTE

1. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.
2. ODT pin driven to a valid state; MR5 [5] = 0 (normal setting).

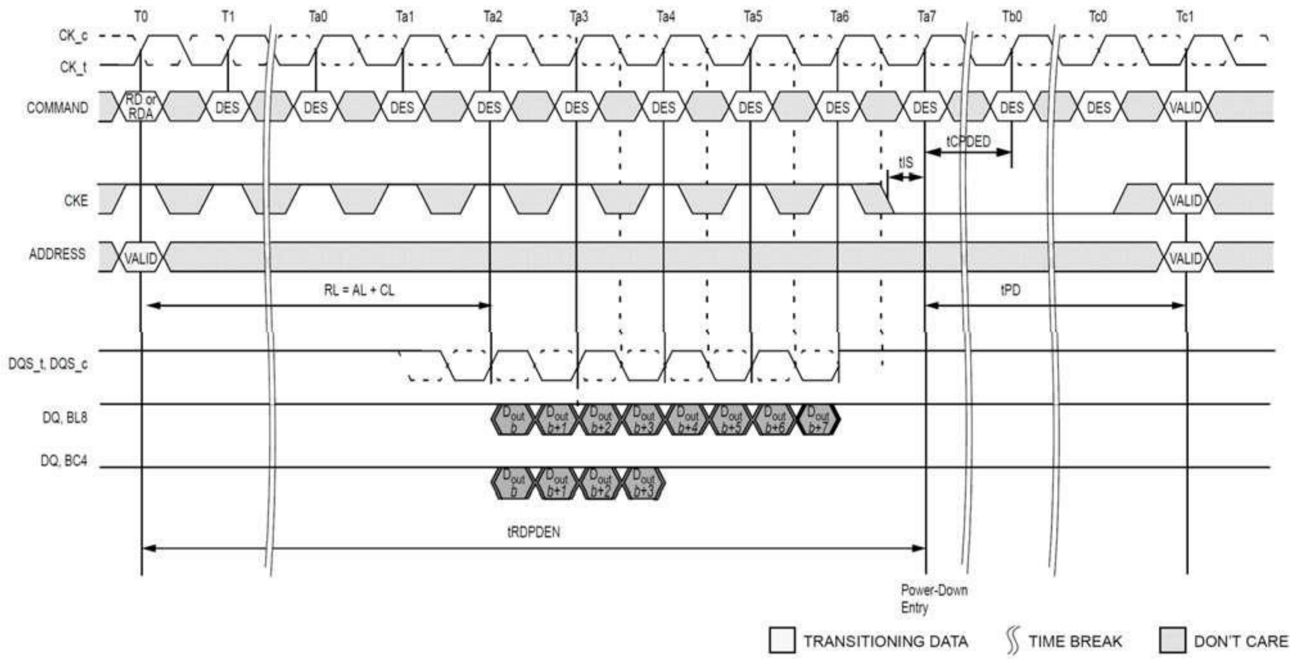
Active Power-Down Entry and Exit Timing Diagram (MR5 bit A5=1)



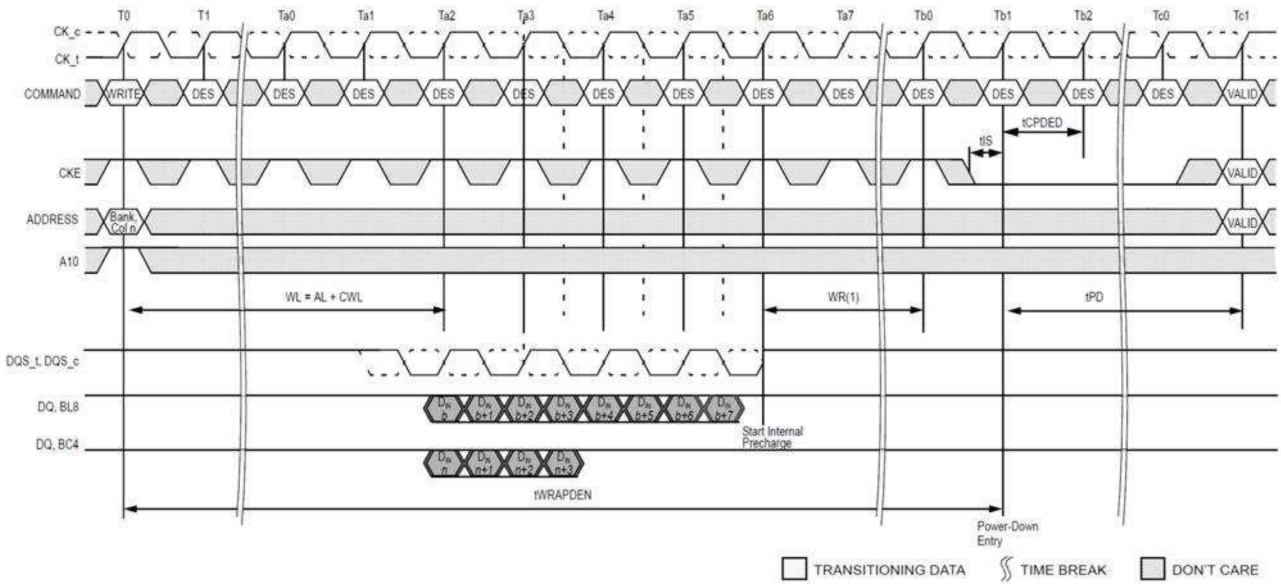
NOTE

1. Valid commands at T0 are ACT, DES, or PRE with one bank remaining open after completion of the PRECHARGE command.
2. ODT pin driven to a valid state; MR5 [5] = 1.

Power-Down Entry after Read and Read with Auto Precharge

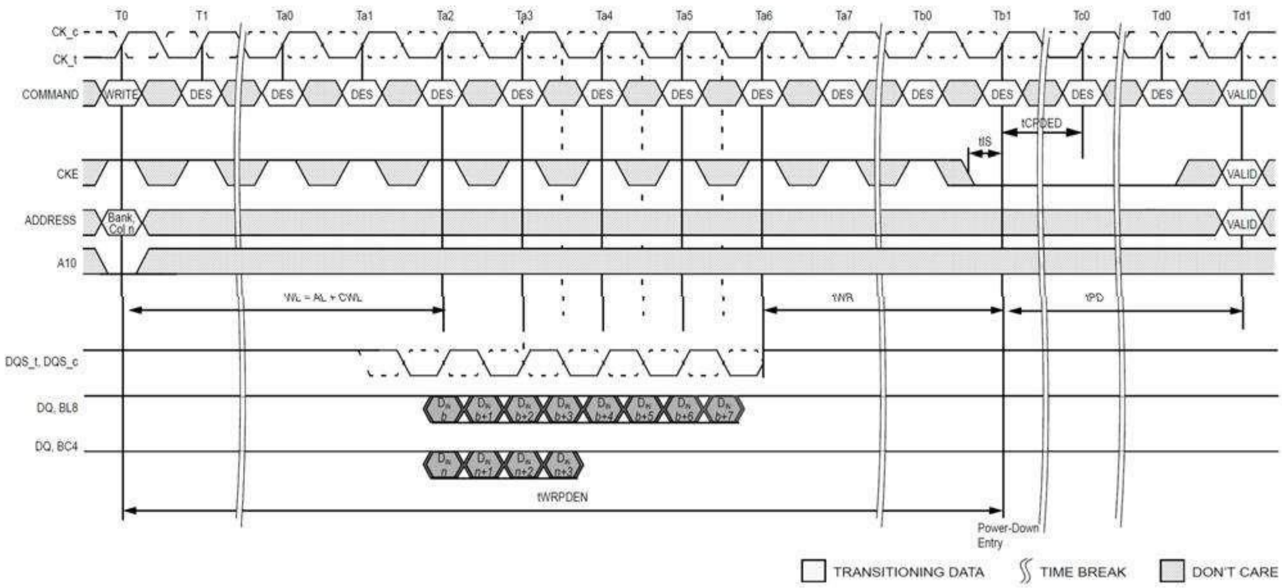


Power-Down Entry After Write with Auto Precharge

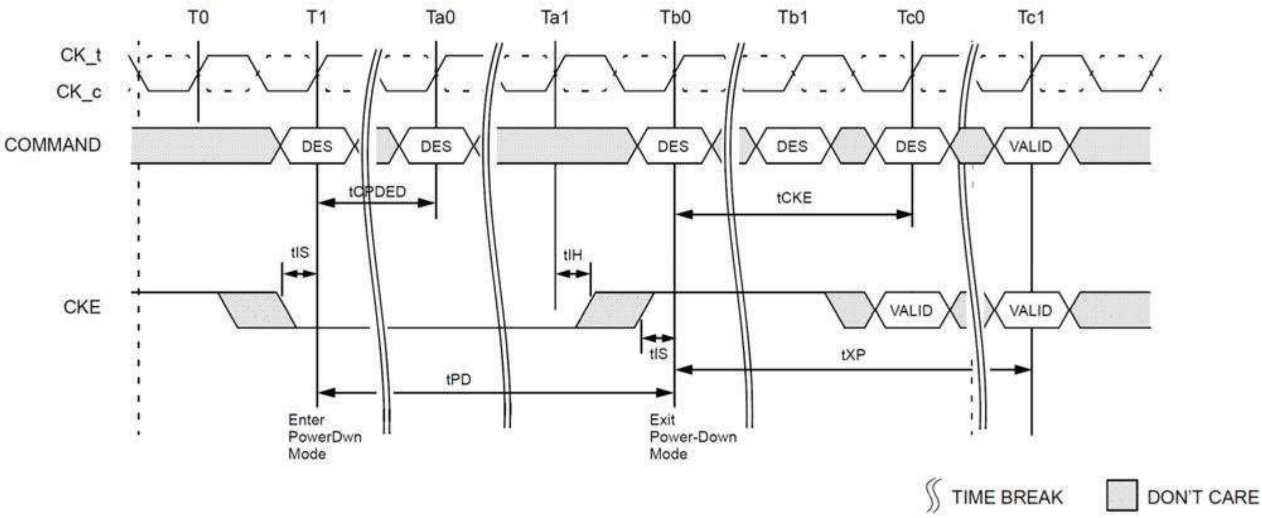


NOTE 1. tWR is programmed through MR0.

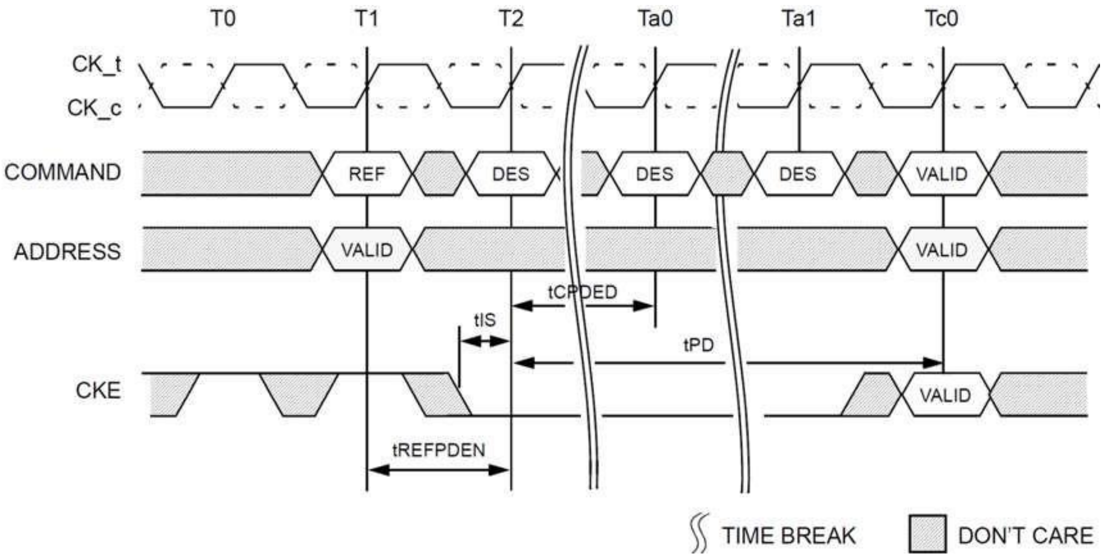
Power-Down Entry after Write



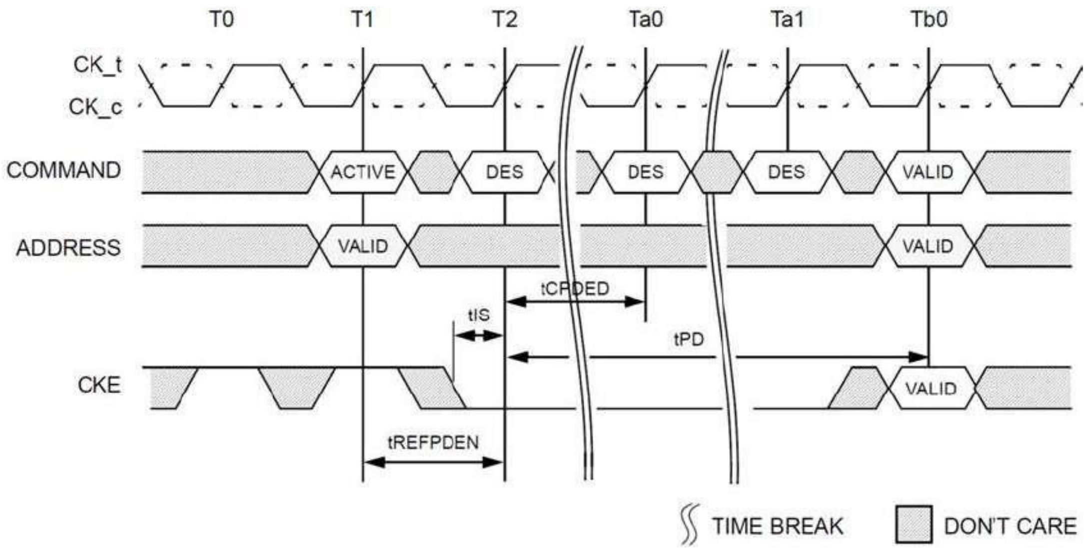
Precharge Power-Down Entry and Exit



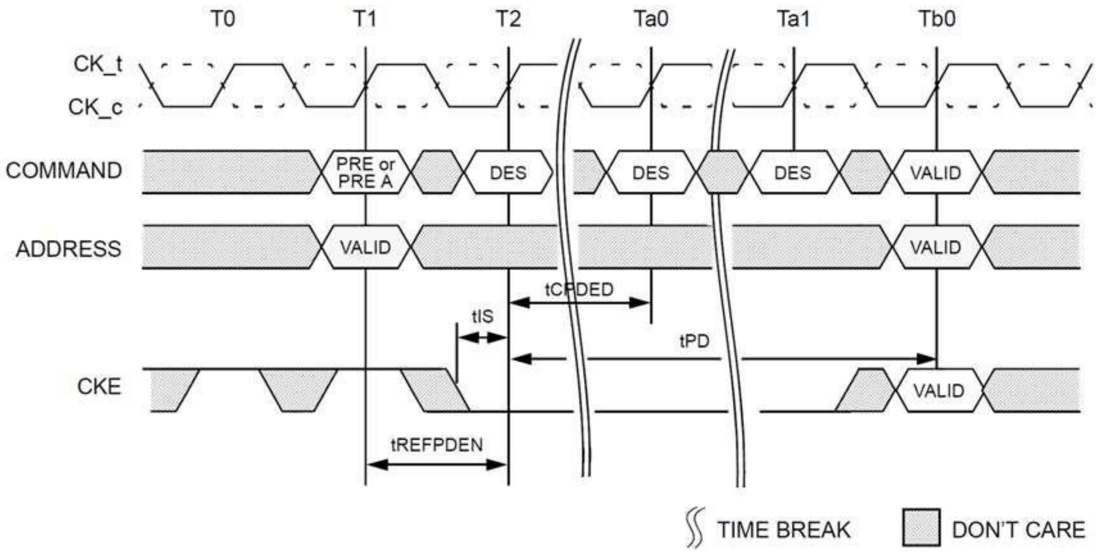
Refresh Command to Power-Down Entry



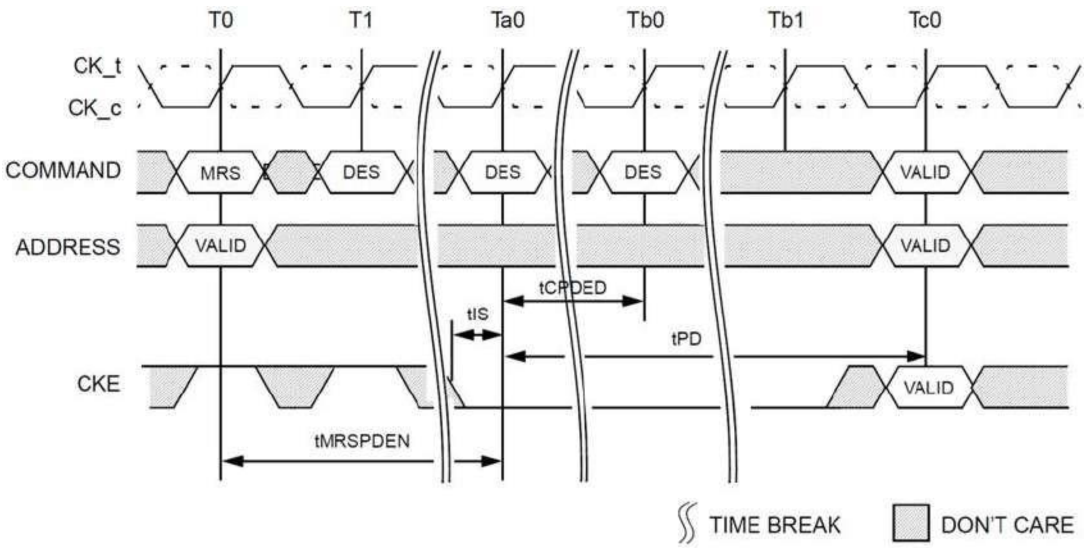
Activate Command to Power-Down Entry



Precharge/Precharge all Command to Power-Down Entry



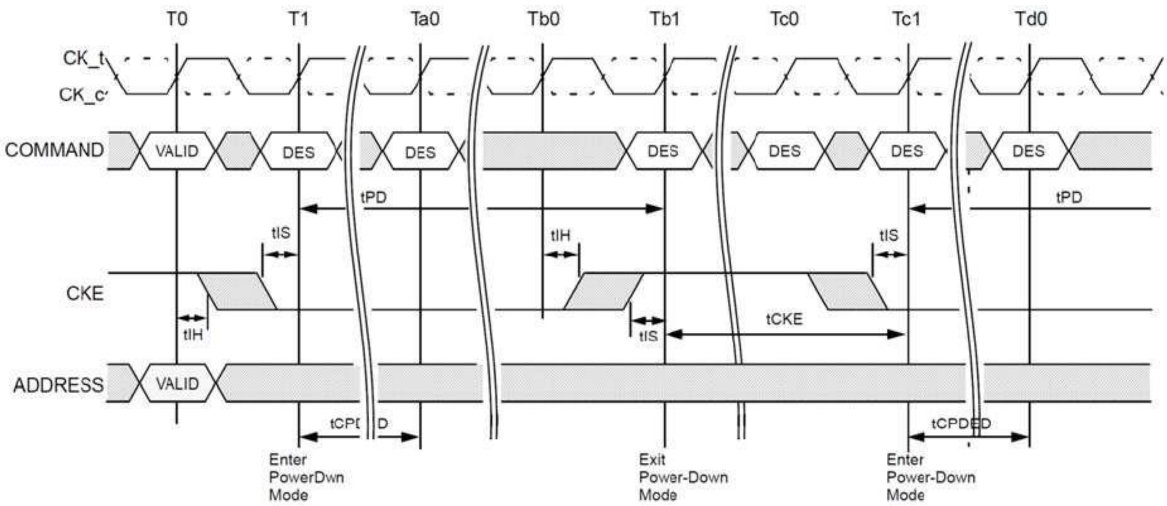
MRS Command to Power-Down Entry



Power-Down Clarifications

When CKE is registered LOW for power-down entry, tPD (MIN) must be satisfied before CKE can be registered HIGH for power-down exit. The minimum value of parameter tPD (MIN) is equal to the minimum value of parameter tCKE (MIN) as shown in the Timing Parameters by Speed Bin table. A detailed example of Case 1 is shown below.

Power-Down Entry/Exit Clarification



Maximum Power Saving Mode

This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting RESET_n signal LOW) to minimize the power consumption.

Maximum Power-Saving Mode Entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command. Note that large CS_n hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

Maximum Power Saving mode Entry

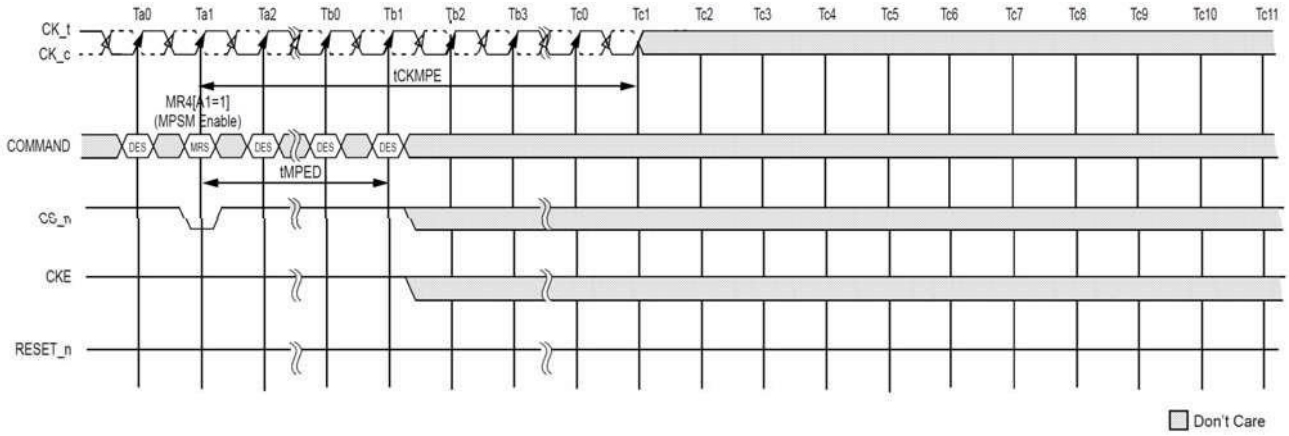
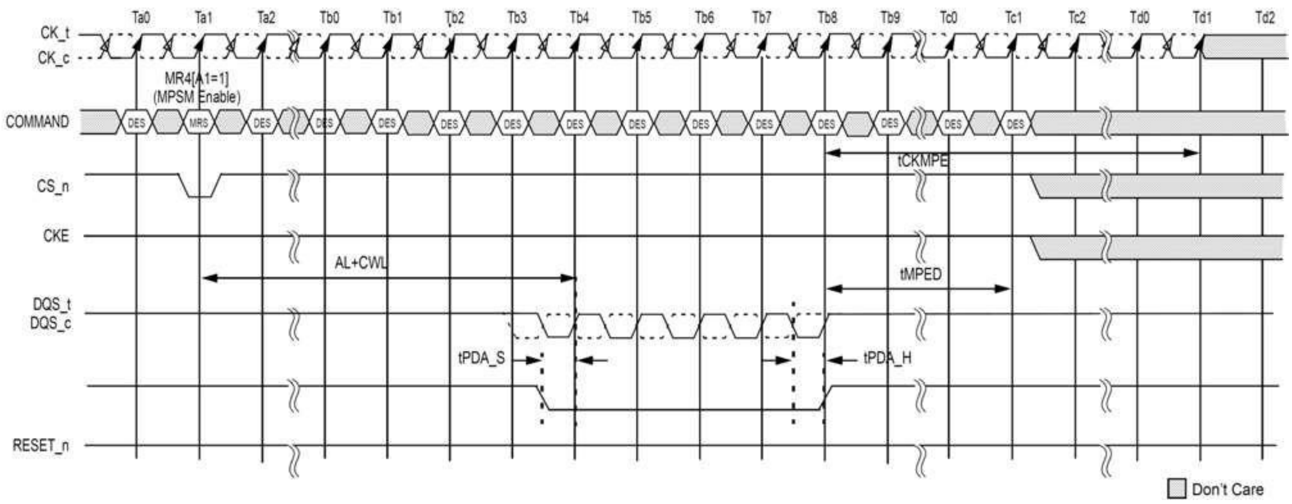


Figure below illustrates the sequence and timing parameters required for the maximum power saving mode with the per DRAM addressability (PDA).

Maximum Power Saving mode Entry with PDA

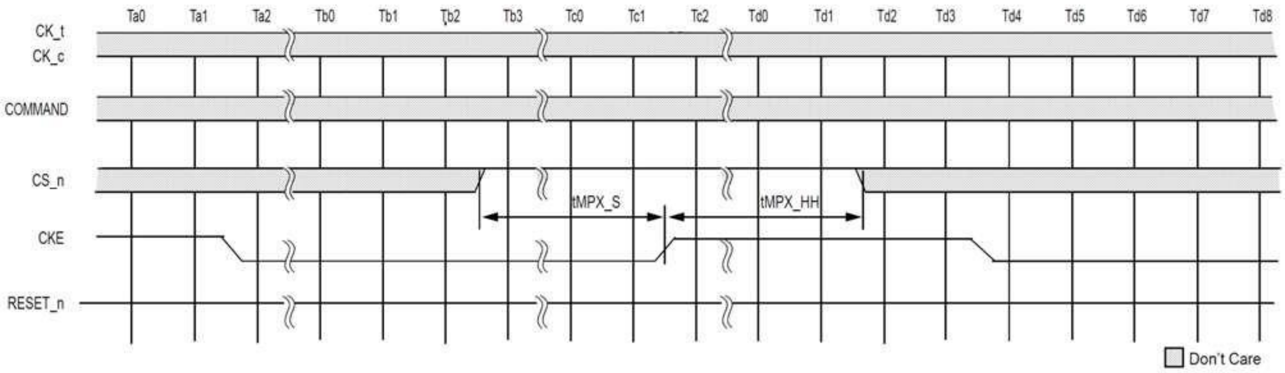


When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except CS_n, CKE and RESET_n signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

CKE Transition during Maximum Power-Saving Mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, CS_n should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

CKE Transition Limitation to hold Maximum Power Saving Mode

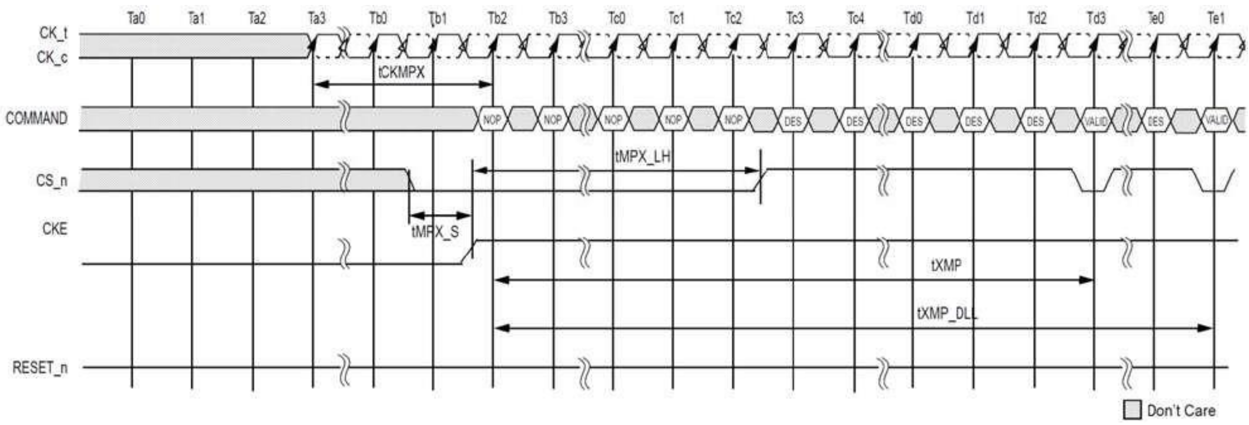


Maximum Power-Saving Mode Exit

DRAM monitors CS_n signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the CS_n signal level at the CKE transition. Because CK receivers are shut down during this mode, CS_n ='L' is captured by rising edge of the CKE signal. If CS_n signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 [A1] is move to '0' automatically.

Maximum Power Saving Mode Exit Sequence



Timing parameter bin of Maximum Power Saving Mode for DDR4-1600/1866/2133/2400/2666/3200

Description	Symbol	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	Note
		Min	Max	Min	Max		
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	CK	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	CK	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	tCKSRX(min)	-	CK	
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	CK	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)	-	CK	
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	CK	
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)	-	tXP(min)	-	CK	
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	12	tXMP-10ns	ns	1

NOTE 1 tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

Connectivity Test Mode

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independant of density and optional for all x8 and x4 width devices with densities greater than or equal to 8Gb.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. RESET_n is registered to High and VrefCA must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the

DDR4 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be tri-stated. The CS_n pin in the DDR4 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.
4. Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. RESET_n : Fixed high level is required during CT mode same as normal function.

Pin Classification of DDR4 Memory Device in Connectivity Test (CT) Mode

CT Mode Pins		Pin Names during Normal Memory Operation
Test Enable		TEN
Chip Select		CS_n
Test Input	A	BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, CKE, ACT_n, ODT, CLK_t, CLK_c, Parity
	B	DML_n, DBIL_n, DMU_n/DBIU_n, DM_n/DBI_n
	C	Alert_n
	D	RESET_n
Test Output		DQ0-DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c

Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e, 960mV for DC high and 240mV for DC low.

Min Terms Definition for Logic Equations

Min Term Equations

MTx is an inernal signal to be used to generate the signal to drive the output signals.

MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT, A9)
MT2 = XOR (A2, A5, A15)
MT3 = XOR (A0 A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n)
MT5 = XOR (Cke, RAS_n,/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = XOR (((x16 and DMU_n / DBIU_n) or (!x16 and BG1)), ((x8 or x16) and DML_n / DBIL_n), CK_t))
MT8 = XOR (WE_n / A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, (Reset_n and TEN))

Output equations for x4 devices

DQ0 = XOR(MT0, MT1)
DQ1 = XOR(MT2, MT3)
DQ2 = XOR(MT4, MT5
DQ3 = XOR(MT6, MT7)
DQS_t = MT8
DQS_c = MT9

Output equations for x8 devices

DQ0 = MT0
DQ1 = MT1
DQ2 = MT2
DQ3 = MT3
DQ4 = MT4
DQ5 = MT5
DQ6 = MT6
DQ7 = MT7
DQS_t = MT8
DQS_c = MT9

Output equations for x16 devices

DQ0 = MT0
DQ1 = !DQ0
DQ2 = MT1
DQ3 = !DQ2
DQ4 = MT2
DQ5 = !DQ4
DQ6 = MT3
DQ7 = !DQ6
DQ8 = MT4
DQ9 = !DQ8
DQ10 = MT5
DQ11 = ! DQ10
DQ12 = MT6
DQ13 = MT7
DQ14 = MT8
DQ15 = !DQ14
DQSL_t = MT9
DQSL_c = !DQ12
DQSU_t = !DQSL_t
DQSU_c = !DQ13

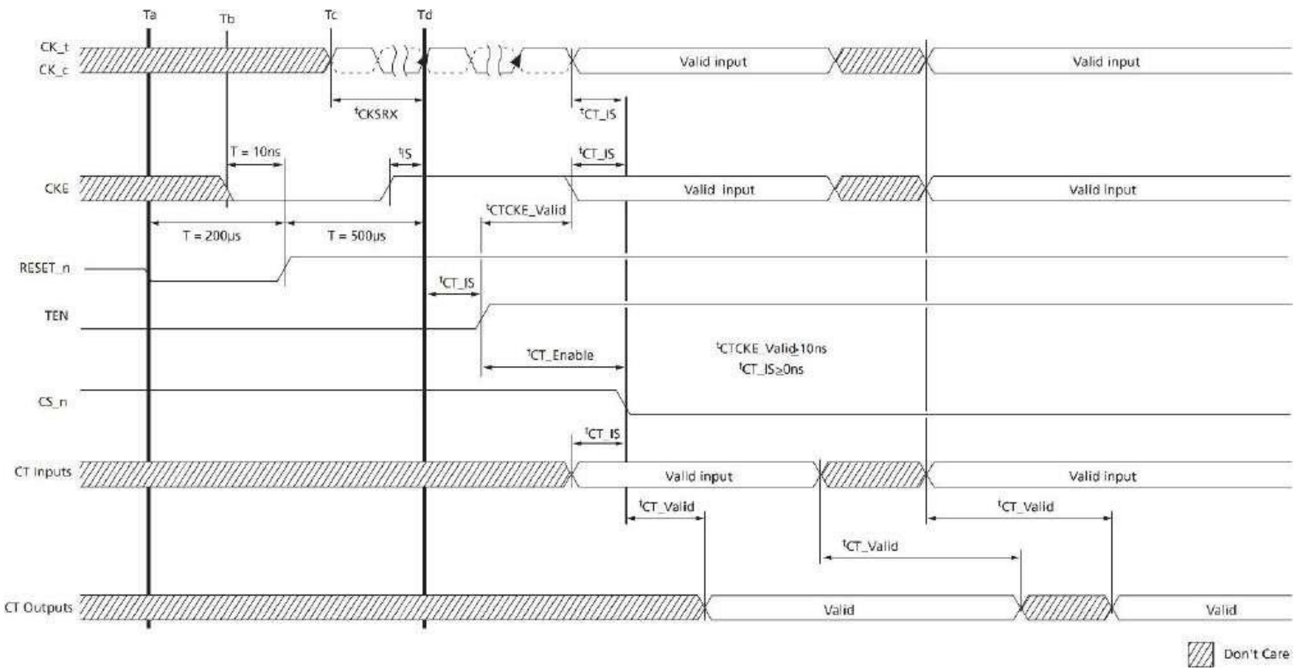
CT Input Timing Requirement

Prior to the assertion of the TEN pin, all voltage supplies, including VREFCA, must be valid and stable and RESET_n registered high prior to entering CT mode. Upon the assertion of the TEN pin HIGH with RESET_n, CKE, and CS_n held HIGH; CLK_t, CLK_c, and CKE signals become test inputs within tCTECT_Valid. The remaining CT inputs become valid tCT_Enable after TEN goes HIGH when CS_n allows input to begin sampling, provided inputs were valid for at least tCT_Valid. While in CT mode, refresh activities in the memory arrays are not allowed; they are initiated either externally (auto refresh) or internally (self refresh).

The TEN pin may be asserted after the DRAM has completed power-on. After the DRAM is initialized and VREFDQ is calibrated, CT mode may no longer be used. The TEN pin may be de-asserted at any time in CT mode. Upon exiting CT mode, the states and the integrity of the original content of the memory array are unknown. A full reset of the memory device is required.

After CT mode has been entered, the output signals will be stable within tCT_Valid after the test inputs have been applied as long as TEN is maintained HIGH and CS_n is maintained LOW.

Connectivity Test Mode Entry



Symbol	Min	Max	Unit
tCT_IS	0	-	ns
tCT_Enable	200	-	ns
tCT_Valid	-	200	ns

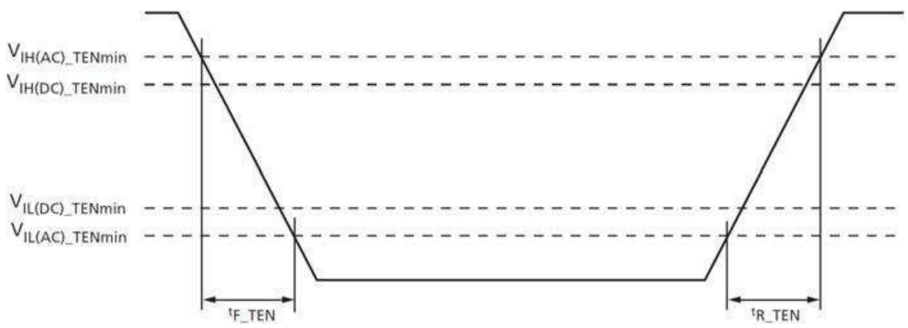
CT Input Levels

CMOS rail to rail Input Levels for TEN

Symbol	Parameter	Min	Max	Unit	Note
VIH(AC)_TEN	TEN AC Input High Voltage	0.8 x VDD	VDD	V	1
VIH(DC)_TEN	TEN DC Input High Voltage	0.7 x VDD	VDD	V	
VIL(DC)_TEN	TEN DC Input Low Voltage	VSS	0.3 x VDD	V	
VIL(AC)_TEN	TEN AC Input Low Voltage	VSS	0.2 x VDD	V	2
TF_input_TEN	TEN Input signal Falling time	–	10	ns	
TR_input_TEN	TEN Input signal Rising time	–	10	ns	

NOTE
1. Overshoot should not exceed the Vin Absolute Maximum Ratings.
2. Undershoot should not exceed the Vin Absolute Maximum Ratings.

TEN Input Slew Rate Definition

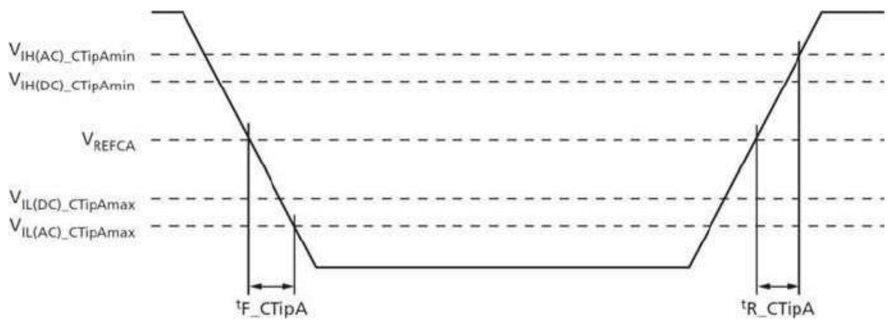


CT Type-A Input Levels

Parameter	Symbol	Min	Mix	Unit	Note
CTipA AC Input High Voltage	VIH(AC)_CTipA	VREFCA + 0.2	Note [1]	V	
CTipA DC Input High Voltage	VIH(DC)_CTipA	VREFCA + 0.15	VDD	V	
CTipA DC Input Low Voltage	VIL(DC)_CTipA	VSS	VREFCA - 0.15	V	
CTipA AC Input Low Voltage	VIL(AC)_CTipA	Note [1]	VREFCA - 0.2	V	
CTipA Input signal Falling time	TF_input_CTipA	-	5	ns	
CTipA Input signal Rising time	TR_input_CTipA	-	5	ns	

NOTE 1 See “Overshoot and Undershoot Specifications”.

CT Type-A Input Slew Rate Definition

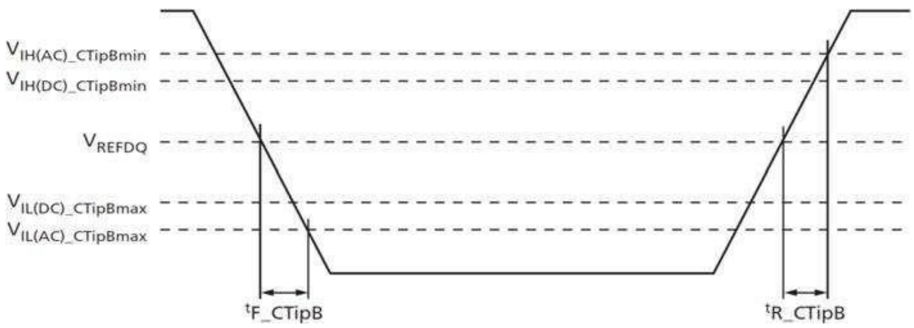


CT Type-B Input Levels

Parameter	Symbol	Min	Mix	Unit	Note
CTipB AC Input High Voltage	VIH(AC)_CTipB	VREFDQ + 0.3	Note 2	V	1
CTipB DC Input High Voltage	VIH(DC)_CTipB	VREFDQ + 0.2	VDDQ	V	1
CTipB DC Input Low Voltage	VIL(DC)_CTipB	VSSQ	VREFDQ - 0.2	V	1
CTipB AC Input Low Voltage	VIL(AC)_CTipB	Note 2	VREFDQ - 0.3	V	1
CTipB Input signal Falling time	TF_input_CTipB	-	5	ns	
CTipB Input signal Rising time	TR_input_CTipB	-	5	ns	

NOTE
1. VREFDQ is VDDQ*0.5.
2. See "Overshoot and Undershoot Specifications".

CT Type-B Input Slew Rate Definition

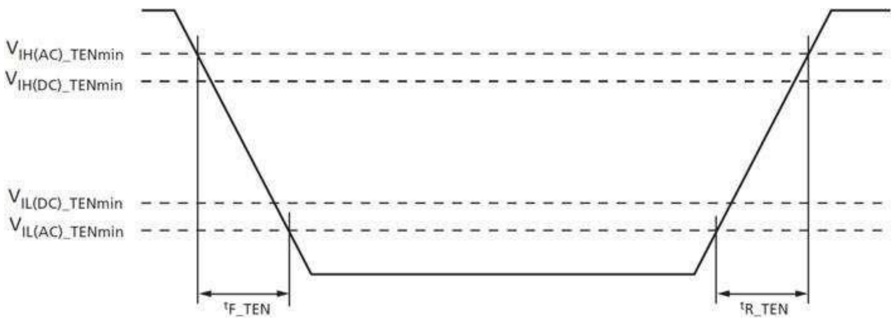


CT Type-C Input Levels (CMOS)

Parameter	Symbol	Min	Mix	Unit	Note
CTipC AC Input High Voltage	VIH(AC)_CTipC	0.8 × VDD	VDD [1]	V	2
CTipC DC Input High Voltage	VIH(DC)_CTipC	0.7 × VDD	VDD	V	2
CTipC DC Input Low Voltage	VIL(DC)_CTipC	VSS	0.3 × VDD	V	2
CTipC AC Input Low Voltage	VIL(AC)_CTipC	VSS [1]	0.2 × VDD	V	2
CTipC Input signal Falling time	TF_input_CTipC	-	10	ns	2
CTipC Input signal Rising time	TR_input_CTipC	-	10	ns	2

NOTE
1. Refer to Overshoot and Undershoot Specifications.
2. CT Type-C inputs: Alert_n.

CT Type-C Input Slew Rate Definition



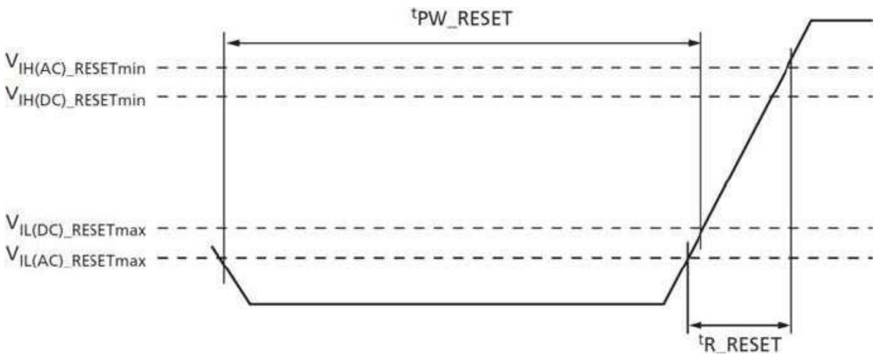
CT Type-D Input Levels

Parameter	Symbol	Min	Mix	Unit	Note
CTipD AC Input High Voltage	VIH(AC)_CTipD	0.8 × VDD	VDD	V	4
CTipD DC Input High Voltage	VIH(DC)_CTipD	0.7 × VDD	VDD	V	2
CTipD DC Input Low Voltage	VIL(DC)_CTipD	VSS	0.3 × VDD	V	1
CTipD AC Input Low Voltage	VIL(AC)_CTipD	VSS	0.2 × VDD	V	5
Rising time	tR_RESET	-	1	µs	3
RESET pulse width - after power-up	tPW_RESET_S	1	-	µs	2
RESET pulse width - during power-up	PW_RESET_L	200	-	µs	2

NOTE

1. After RESET_n is registered LOW, the RESET_n level must be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, the DRAM may not be reset.
2. After RESET_n is registered HIGH, the RESET_n level must be maintained above VIH(DC)_RESET, otherwise, operation will be uncertain until it is reset by asserting RESET_n signal LOW.
3. Slope reversal (ring-back) during this level transition from LOW to HIGH should be mitigated as much as possible.
4. Overshoot should not exceed the VIN values in the Absolute Maximum Ratings table.
5. Undershoot should not exceed the VIN values in the Absolute Maximum Ratings table.
6. CT Type-D inputs: RESET_n; same requirements as in normal mode.

CT Type-D Input Slew Rate Definition



CLK to Read DQS Timing Parameters

DDR4 supports DLLOFF mode. Following parameters will be defined for CK to read DQS timings.

Speed		DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Note
Parameter	Symbol	Min	Max		
DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c	tDQSCK (DLL On)	refer to AC parameter tables	refer to AC parameter tables	ps	1,3,8,9
	tDQSCK (DLL Off)	vendor specific	vendor specific	ps	2, 3, 8
DQS_t, DQS_c rising edge output variance window	tDQSCKi(DLL On)	-	refer to AC parameter tables	ps	1,5,6,8,9
	tDQSCKi(DLL Off)	-	vendor specific	ps	2,4,5,6,8
VDD sensitivity of tDQSCK (DLL Off)	dTDQSCKdV	-	vendor specific	ps/mV	2, 6
Temperature sensitivity of tDQSCK (DLL Off)	dTDQSCKdT	-	vendor specific	ps/oC	2,6

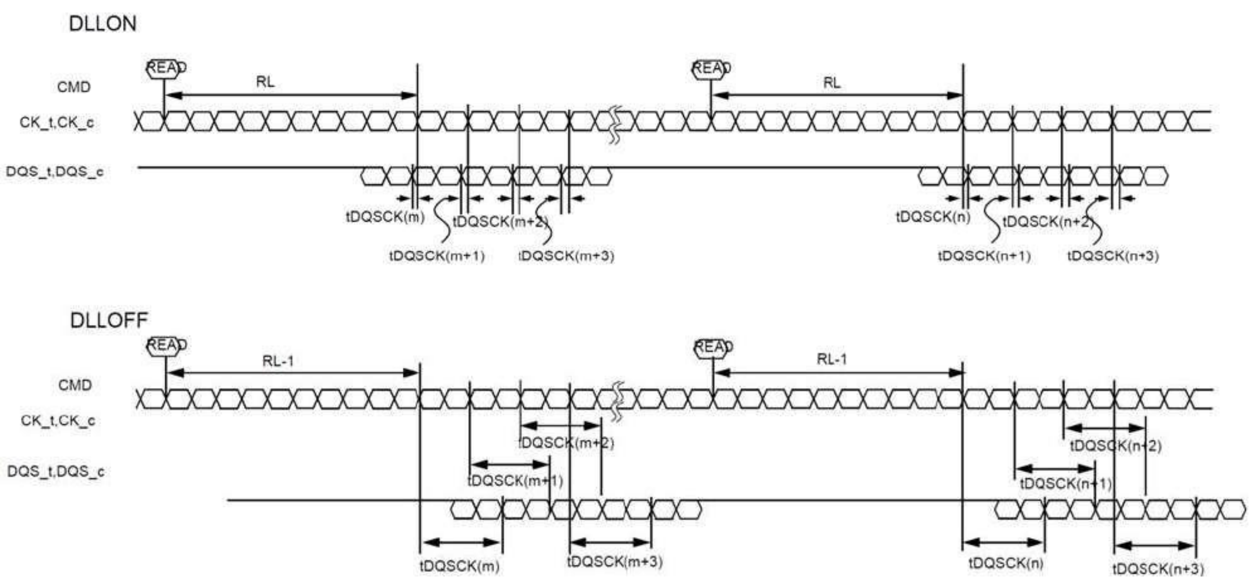
NOTE
1. These parameters are applied when DRAM is in DLLON mode.
2. These parameters are applied when DRAM is in DLLOFF mode.
3. Measured over full VDD and Temperature spec ranges.
4. Measured at fixed and constant VDD and Temperature condition.
5. Measured for a given DRAM part, and for each DQS/DQ pair in case of x16 (part variation is excluded).
6. These parameters are verified by design and characterization, and may not be subject to production test.
7. Assume no jitter on input clock signals to the DRAM.
8. Refer to “READ Timing Definitions”.
9. Refer to READ Timing Definitions READ Timing Definitions.

tDQSCK,Min
= Min {Min {tDQSCK(j), all VDD and Temperature ranges}, all DQS pairs and parts}

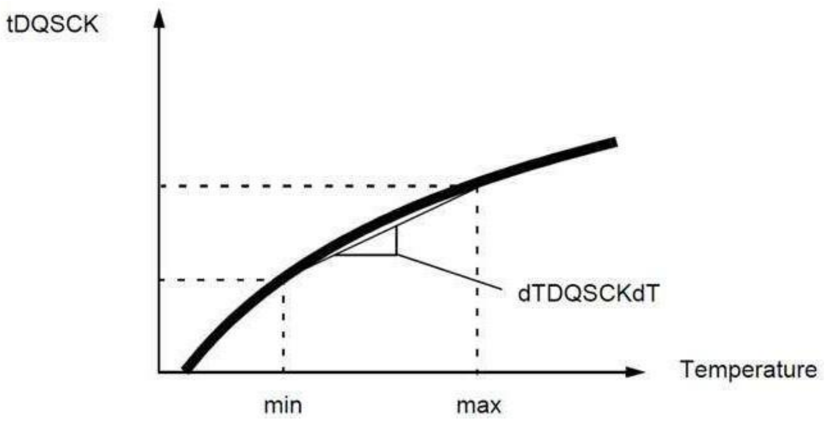
tDQSCK,Max
= Max {Max {tDQSCK(j), all VDD and Temperature ranges}, all DQS pairs and parts}

tDQSCKJ, Max
= Max {tDQSCK(j), fixed VDD and Temperature} - Min {tDQSCK(j), fixed VDD and Temperature}

tDQSCK Definition Difference between DLL ON and DLL OFF

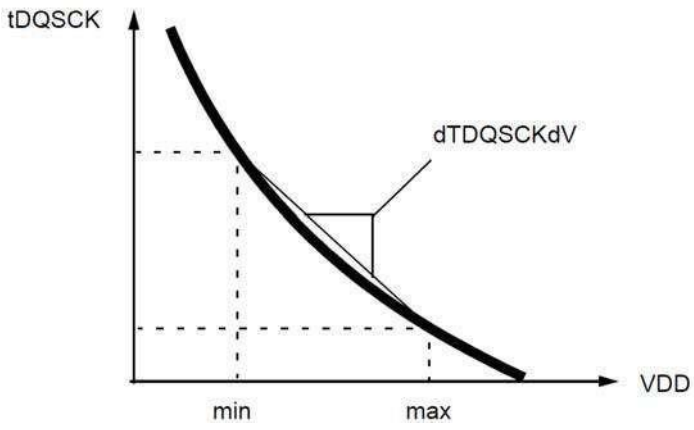


dTDQSCKTdT Definition



dTDQSCKdT = l tDQSCK(Toper,max) - tDQSCK(Toper,min)l / lToper,max - Toper,minl

TDQSCKTdV Definition



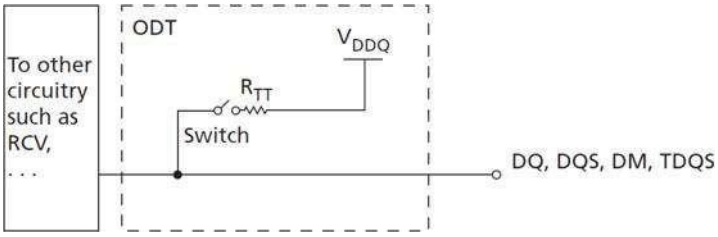
dTDQSCKdV = l tDQSCK(VDD,max) - tDQSCK(VDD,min)l / lVDD,max - VDD,minl

On-Die Termination (ODT)

The on-die termination (ODT) feature enables the device to change termination resistance for each DQ, DQS, and DM_n/DBI_n signal for x4 and x8 configurations (and TDQS for the x8 configuration when enabled via A11 = 1 in MR1) via the ODT control pin, WRITE command, or default parking value with MR setting. For the x16 configuration, ODT is applied to each UDQ, LDQ, UDQS, LDQS, UDM_n/UDBI_n, and LDM_n/LDBI_n signal. The ODT feature is designed to improve the signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. If DBI read mode is enabled while the DRAM is in standby, either DM mode or DBI write mode must also be enabled if RTT(NOM) or RTT(Park) is desired. More details about ODT control modes and ODT timing modes can be found further along in this document.

The ODT feature is turned off and not supported in self refresh mode.

Functional Representation of ODT



The switch is enabled by the internal ODT control logic, which uses the external ODT pin and other control information. The value of RTT is determined by the settings of mode register bits (see Mode Register). The ODT pin will be ignored if the mode register MR1 is programmed to disable RTT(NOM) [MR1[10,9,8] = 0,0,0] and in self refresh mode.

ODT Mode Register and ODT State Table

The ODT Mode of DDR4 SDRAM has 4 states, Data Termination Disable, RTT_WR, RTT_NOM and RTT_PARK. And the ODT Mode is enabled if any of MR1{A10,A9,A8} or MR2 {A10:A9} or MR5 {A8:A6} are non zero. In this case, the value of RTT is determined by the settings of those bits.

After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and ODT pin

- RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW)
- RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except ODT is disabled by MR1).
- RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X + Y clock cycles.

  X is 2 for 1tCK and 3 for 2tCK preamble mode.

  Y is 0 when CRC is disabled and 1 when it's enabled
- The Termination State Table is shown in Table 54.

Those RTT values have following priority.

1. Data Termination Disable
2. RTT_WR
3. RTT_NOM
4. RTT_PARK

which means if there is WRITE command along with ODT pin HIGH, then DRAM turns on RTT_WR not RTT_NOM, and also if there is READ command, then DRAM disables data termination regardless of ODT pin and goes into Driving mode.

Termination State Table

RTT_PARK MR5{A8:A6}	RTT_NOM MR1 {A10:A9:A8}	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care	RTT_PARK	1,2,3
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care	Hi-Z	1,2,3

NOTE

1. When read command is executed, DRAM termination state will be Hi-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM. This is described in section 1.2.3 ODT During Read.
2. If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM. This is described in section 1.3 Dynamic ODT.
3. If RTT_NOM MRS is disabled, ODT receiver power will be turned off to save power.

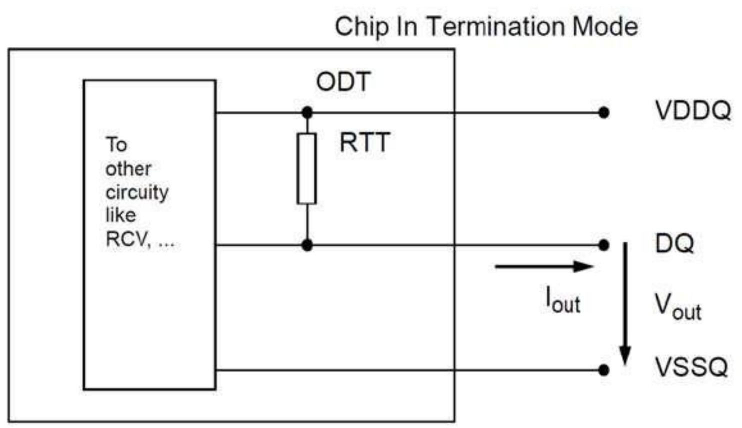
On-Die Termination effective resistance RTT is defined by MRS bits.

ODT is applied to the DQ, DM, DQS_T/DQS_C and TDQS_T/TDQS_C (x8 devices only) pins.

A functional representation of the on-die termination is shown in the figure below.

On Die Termination

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$



On die termination effective Rtt values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration.

RTT	Vout	Min	Nom	Max	Unit	Note
240 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34 ohm	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	VOMdc= 0.8* VDDQ	0	-	10	%	1,2,4,5,6

NOTE

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearityspec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.
3. The tolerance limits are specified under the condition that VDDQ=VDD and VSSQ=VSS
4. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)
5. RTT variance range ratio to RTTNominal value in a given component, including DQS_T and DQS_C

   DQ-DQ Mismatch in a device = $\frac{RTTmax-RTTmin}{RTTNOM} * 100$

6. This parameter of x16 device is specified for Upper byte and Lower byte.

Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode
- Precharge power down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoff = WL - 2.

When operating in 2tCK Preamble Mode, The ODT latency must be 1 clock smaller than in 1tCK Preamble Mode; DODTLon =WL - 3; DODTLoff = WL - 3."(WL = CWL+AL+PL).

ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register MR1 applies to ODT Latencies as shown below:

ODT Latency

Applicable when write CRC is disabled

Symbol	Parameter	1 tCK Preamble	2 tCK Preamble	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	
RODTLoff	Read command to internal ODT turn off Latency	CWL + AL + PL – 2 CK	CWL + AL + PL – 3 CK	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	RODTLoff + 4	RODTLoff + 5	
RODTLon8	Read command to RTT_PARK turn on Latency in BC8/BL8	RODTLoff + 6	RODTLoff + 7	
ODTH4		4	5	
ODTH8		6	7	

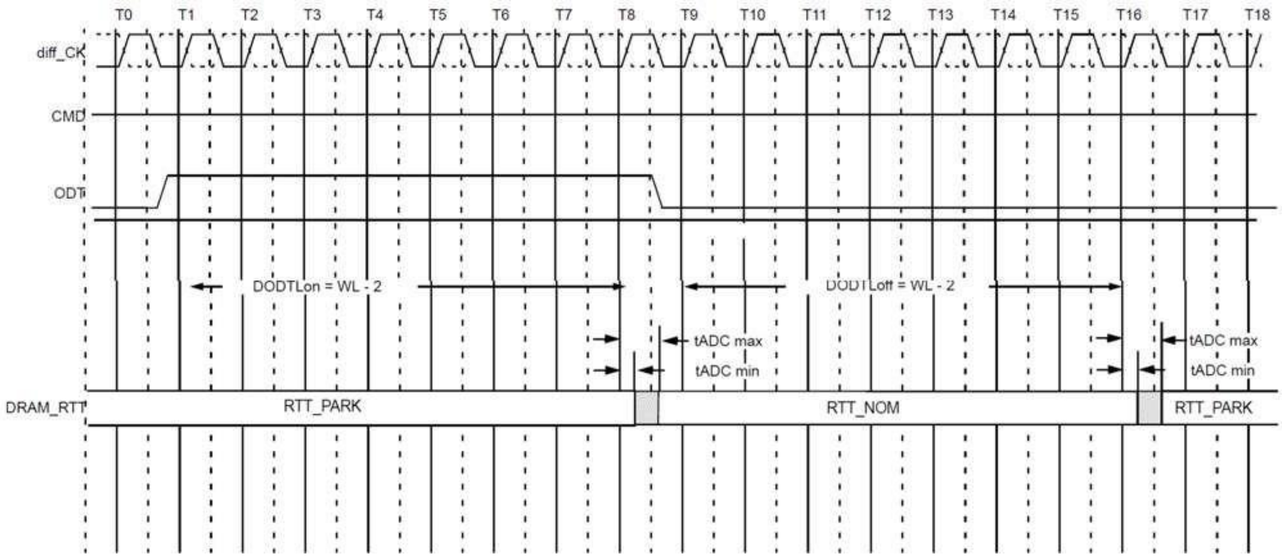
Timing Parameters

In synchronous ODT mode, the following timing parameters apply:

- DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC,min,max.
- tADC,min and tADC,max are minimum and maximum RTT change timing skew between different termination values. Those timing parameters apply to both the Synchronous ODT mode and the Data Termination Disable mode.

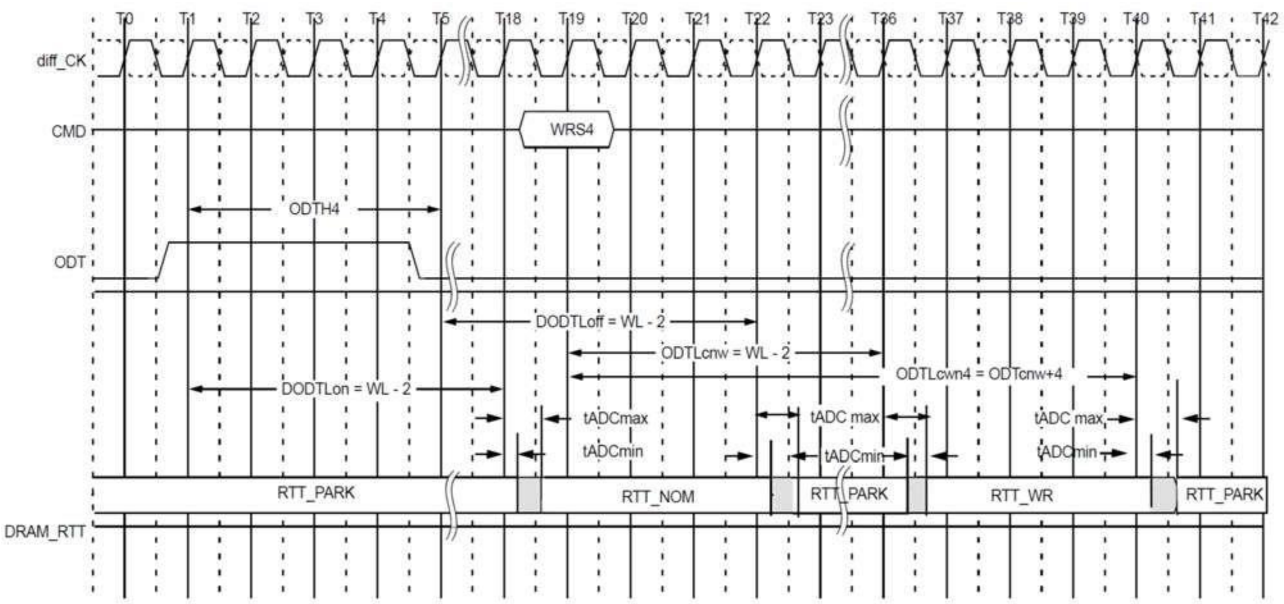
When ODT is asserted, it must remain HIGH until minimum ODTH4 (BL=4) or ODTH8 (BL=8) is satisfied. Additionally, depending on CRC or 2tCK preamble setting in MRS, ODTH should be adjusted.

Synchronous ODT Timing with BL8



Example for CWL = 9, AL = 0, PL = 0; DODTLon = AL + PL +CWL -2 = 7; DODTLoff = AL + PL + CWL -2 = 7.
ODT must be held HIGH for at least ODTH8 after assertion (T1).

Synchronous ODT with BL4



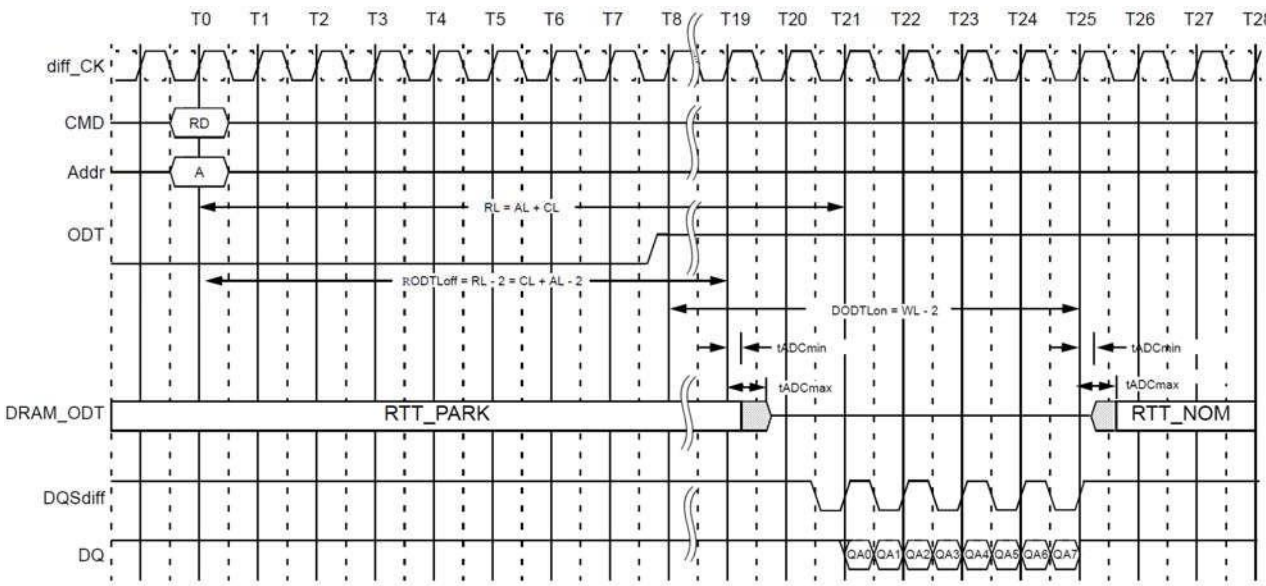
Example for CWL = 9, AL = 10, PL = 0; DODTLon/off = AL + PL+ CWL -2 = 17; ODTcnw = AL + PL+ CWL -2 = 17.

ODT must be held HIGH for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered HIGH to ODT first registered LOW, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or 2tCK preamble setting.

ODT During Reads

Because the DRAM cannot terminate with RTT and drive with RON at the same time, RTT may nominally not be enabled until the end of the postamble as shown in the example below. At cycle T25 the device turns on the termination when it stops driving, which is determined by tHZ. If the DRAM stops driving early (that is, tHZ is early), then tADC (MIN) timing may apply. If the DRAM stops driving late (that is, tHZ is late), then the DRAM complies with tADC (MAX) timing.

Using CL = 11 as an example for the figure below: PL = 0, AL = CL - 1 = 10, RL = PL + AL + CL = 21, CWL= 9; RODTLoff = RL - 2 = 19, DODTLon = PL + AL + CWL - 2 = 17, 1tCK preamble.



Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9;
DODTLon=AL+CWL-2=17; DODTLoff=AL+CWL-2=17;1tCK preamble)

Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR4 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

Functional Description

The Dynamic ODT Mode is enabled if bit A[9] or A[10] of MR2 is set to '1'. The function is described as follows:

- Three RTT values are available: RTT_NOM, RTT_PARK and RTT_WR.
  - The value for RTT_NOM is preselected via bits A[10:8] in MR1
  - The value for RTT_PARK is preselected via bits A[8:6] in MR5
  - The value for RTT_WR is preselected via bits A[10:9] in MR2
- During operation without commands, the termination is controlled as follows;
  - Nominal termination strength RTT_NOM or RTT_PARK is selected.
  - RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff and RTT_PARK is on when ODT is LOW.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_WR is de-selected.
  - 1 or 2 clocks will be added or subtracted into/from ODTLcwn8 and ODTLcwn4 depending on CRC and/or 2tCK preamble setting.

The following table shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The dynamic ODT feature is not supported in DLL-off mode. MRS command must be used to set RTT_WR, MR2[11:9] = 000, to disable dynamic ODT externally.

Dynamic ODT Latencies and Timing (1 tCK Preamble Mode and CRC Disabled)

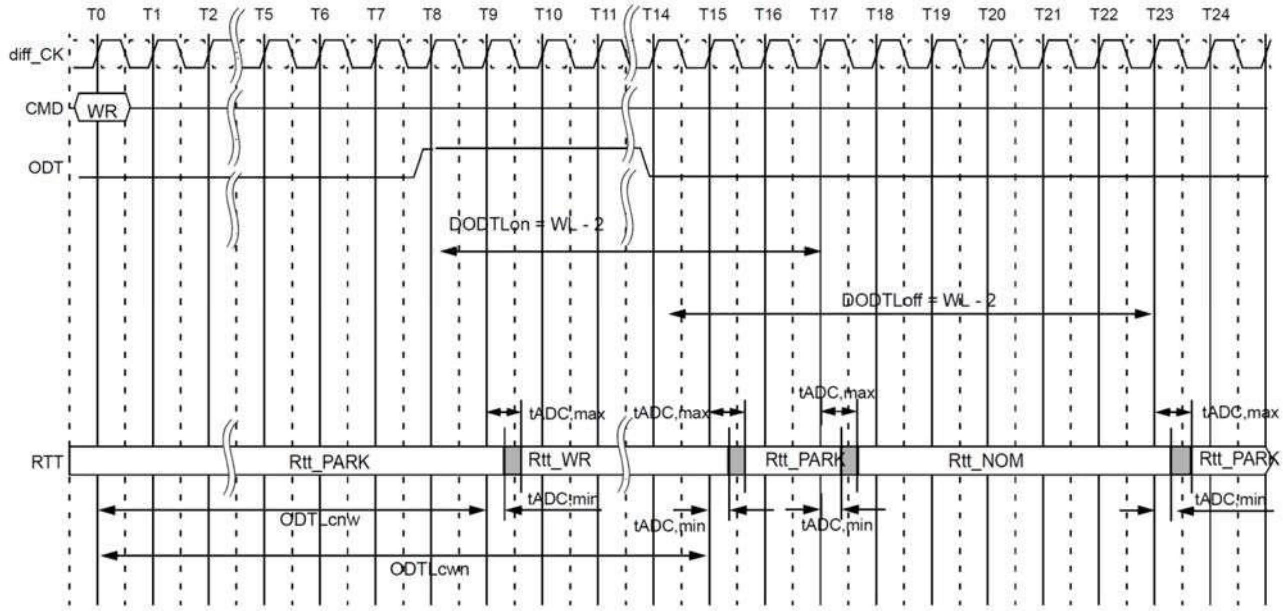
Name and Description	Abbr.	Defined from	Define to	1600/1866/ 2133/2400	2666	2933/3200	Unit
ODT Latency for change from RTT_PARK/ RTT_NOM to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_PARK/ RTT_Nom to RTT_WR	ODTLcnw = WL - 2			tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 4)	ODTLcwn4	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn4 = 4 + ODTLcnw			tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn8 = 6 + ODTLcnw			tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tADC(min) = 0.28 tADC(max) = 0.72	tADC(min) = 0.26 tADC(max) = 0.74	tCK(avg)

Dynamic ODT Latencies and Timing with Preamble Mode and CRC Mode Matrix

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	

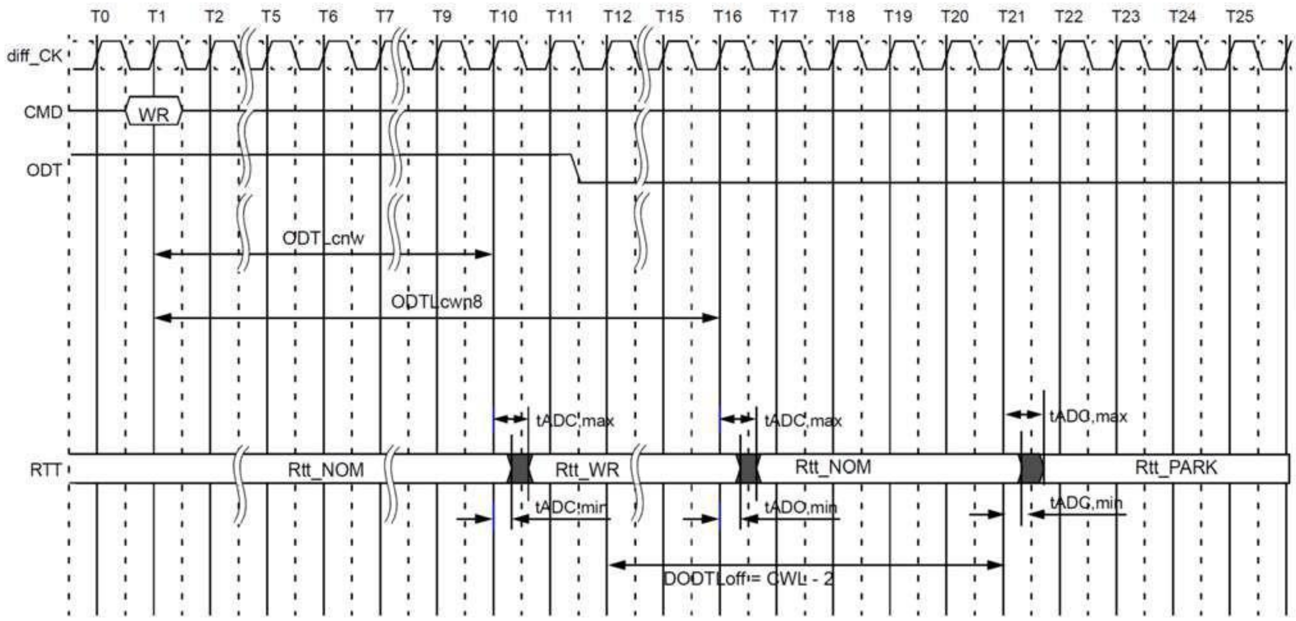
ODT Timing Diagrams

Dynamic ODT (1t CK Preamble; CL = 14, CWL = 11, BL = 8, AL = 0, CRC Disabled)



ODTLcnw = WL-2 (1tCK preamble), WL-3 (2tCK preamble).
ODTLcwn = WL+2 (BC4), WL+4(BL8) w/o CRC or WL+5,5 (BC4, BL8 respectively) when CRC is enabled.

Dynamic ODT Overlapped with RTT_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



Behavior with WR command is issued while ODT being registered high.

Asynchronous ODT mode

Asynchronous ODT mode is selected when DRAM runs in DLL off mode. In asynchronous ODT timing mode, the internal ODT command is *not* delayed by either Additive Latency (AL) or the Parity Latency (PL) relative to the external ODT signal (RTT_NOM).

In asynchronous ODT mode, two timing parameters apply: tAONAS (MIN/MAX), tAOFAS (MIN/MAX).

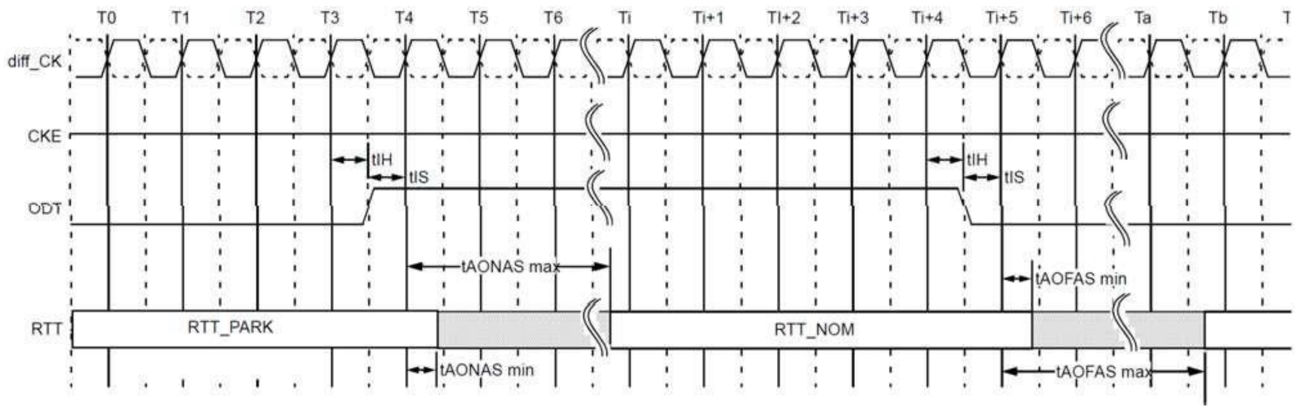
RTT_NOM turn-on time

- Minimum RTT_NOM turn-on time (tAONAS (MIN) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to turn on.
- Maximum RTT_NOM turn-on time (tAONAS [MAX]) is the point in time when the ODT resistance has reached RTT_NOM.
- tAONAS (MIN) and tAONAS (MAX) are measured from ODT being sampled HIGH.

RTT_NOM turn-off time

- Minimum RTT_NOM turn-off time (tAOFAS [MIN]) is the point in time when the device's termination circuit starts to leave RTT_NOM.
- Maximum RTT_NOM turn-off time (tAOFAS [MAX]) is the point in time when the on die termination has reached RTT_PARK.
- tAOFAS (MIN) and tAOFAS (MAX) are measured from ODT being sampled LOW.

Asynchronous ODT Timings with DLL Off



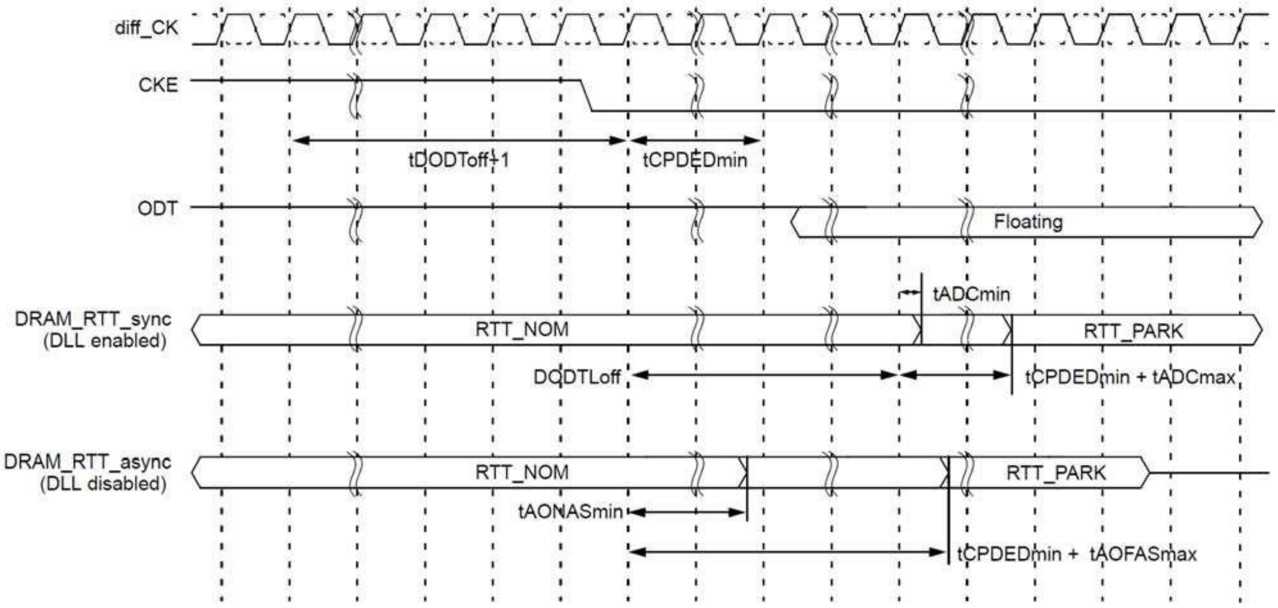
Asynchronous ODT Timing Parameters for all Speed Bins

Description	Symbol	min	max	Unit
Asynchronous RTT turn-on delay	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay	tAOFAS	1.0	9.0	ns

ODT buffer disabled mode for Power down

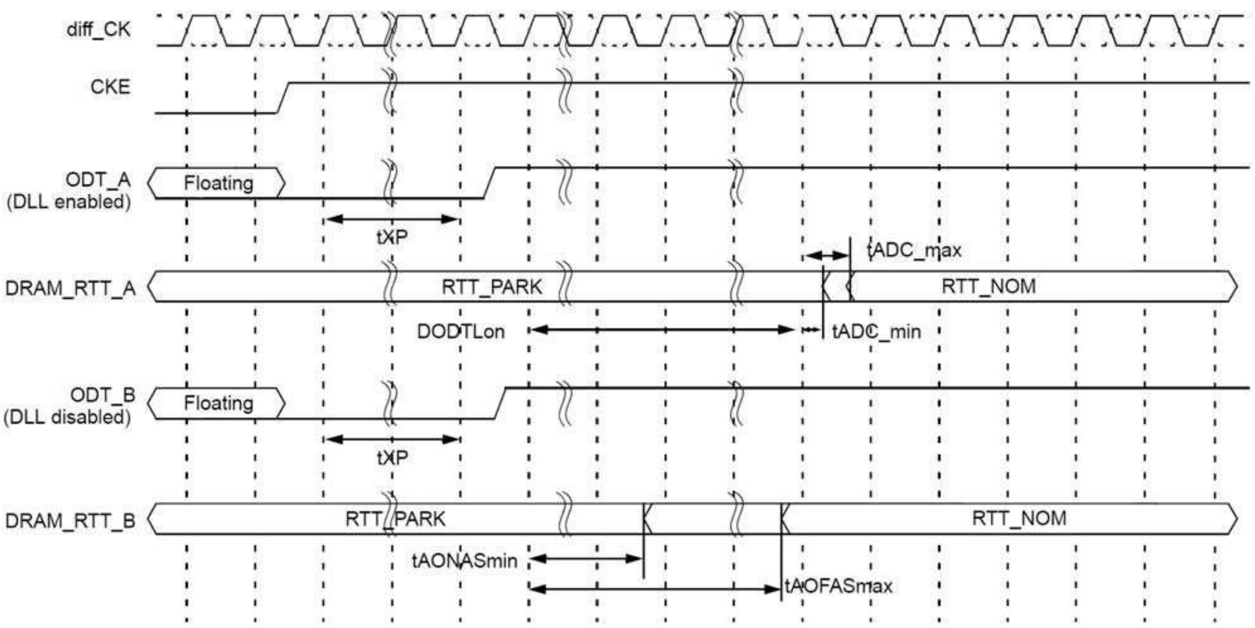
DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

ODT timing for power down entry with ODT buffer disable mode



When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

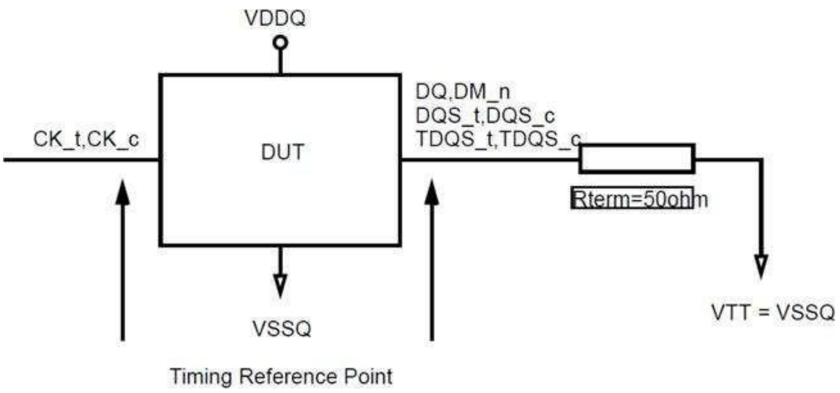
ODT timing for power down exit with ODT buffer disable mode



ODT Timing Definitions

The reference load for ODT timings is different than the reference load used for timing measurements.

ODT Timing Reference Load



ODT Timing Definitions

Definitions for tADC, tAONAS and tAOFAS are provided in the Table and measurement reference settings are provided in the subsequent. The tADC for the Dynamic ODT case and Read Disable ODT cases are represented by tADC of Direct ODT Control case.

ODT Timing Definitions

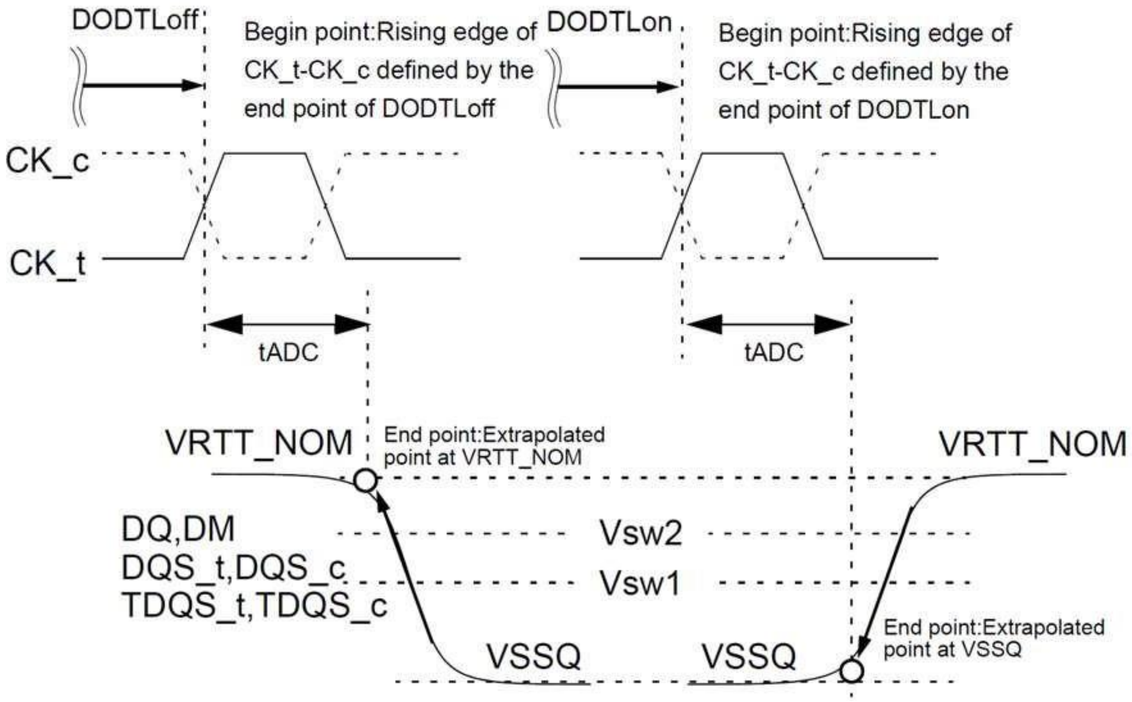
Symbol	Begin Point Definition	End Point Definition
tADC	Rising edge of CK_t,CK_c defined by the end point of DODTLoff	Extrapolated point at VRTT_NOM
	Rising edge of CK_t,CK_c defined by the end point of DODTLon	Extrapolated point at VSSQ
	Rising edge of CK_t,CK_c defined by the end point of ODTLcnw	Extrapolated point at VRTT_NOM
	Rising edge of CK_t,CK_c defined by the end point of ODTLcwn4 or ODTLcwn8	Extrapolated point at VSSQ
tAONAS	Rising edge of CK_t,CK_c with ODT being first registered high	Extrapolated point at VSSQ
tAOFAS	Rising edge of CK_t,CK_c with ODT being first registered low	Extrapolated point at VRTT_NOM

Reference Settings for ODT Timing Measurements

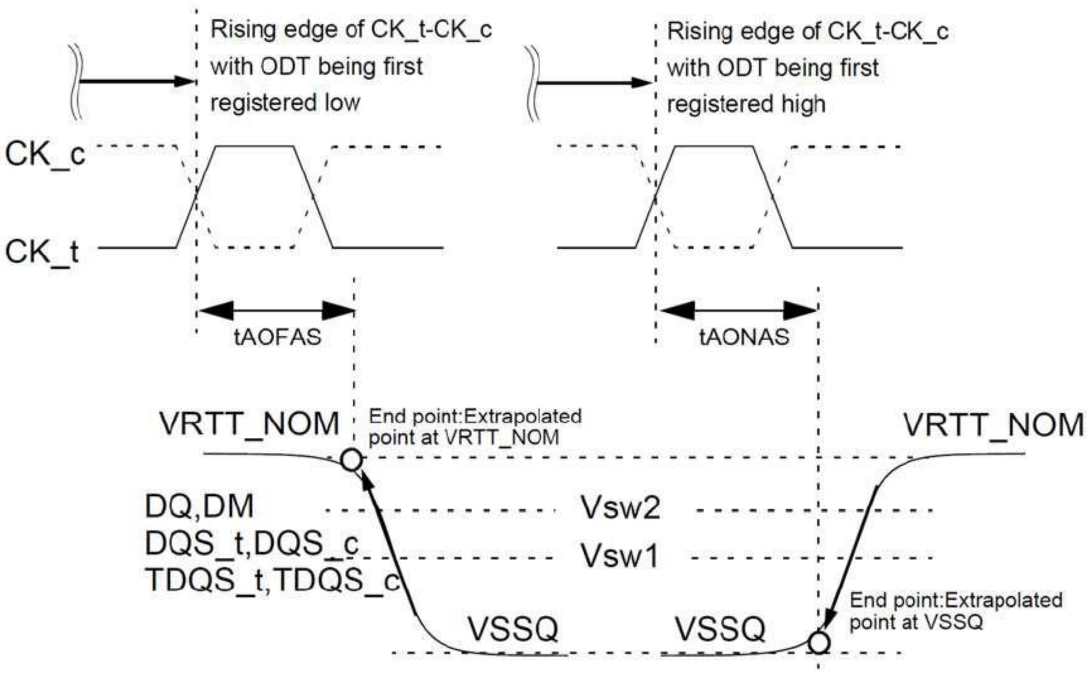
Measured Parameter	RTT_PARK	RTT_NOM	RTT_WR	Vsw1	Vsw2	Note
tADC	Disable	RZQ/7	-	0.20V	0.40V	1,2
	-	RZQ/7	Hi-Z	0.20V	0.40V	1,3
tAONAS	Disable	RZQ/7	-	0.20V	0.40V	1,2
tAOFAS	Disable	RZQ/7	-	0.20V	0.40V	

NOTE
1. MR setting is as follows.
-MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
-MR5 A8=0 , A7=0, A6=0 (RTT_PARK Setting)
-MR2 A11=0, A10=1, A9=1 (RTT_WR Setting)
2. ODT state change is controlled by ODT pin.
3. ODT state change is controlled by Write Command.

Definition of tADC



Definition of tAOFAS and tAONAS



Absolute Maximum DC Ratings

Symbol	Parameter	Min.	Max	Unit	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3	1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3	1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3	3.0	V	4
VIN, VOUT	Voltage on any pin relative to Vss	-0.3	1.5	V	1
TSTG	Storage Temperature	-55	100	°C	1,2

NOTE

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV.
4. VPP must be equal or greater than VDD/VDDQ at all times.

AC and DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The DC bandwidth is limited to 20MHz.

AC and DC Input Measurement Levels

AC & DC Logic input levels for single-ended signals

Single-ended AC & DC input levels for Command and Address

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	NOTE
		min	max	min	max		
VIH.CA(DC75)	DC input logic high	VREF+0.075	VDD			V	
VIL.CA(DC75)	DC input logic low	VSS	VREF-0.075			V	
VIH.CA(DC65)	DC input logic high	-	-	VREF+0.065	VDD	V	
VIL.CA(DC65)	DC input logic low	-	-	VSS	VREF-0.065	V	
VIH.CA(AC100)	AC input logic high	VREF+0.1	Note 2			V	1
VIL.CA(AC100)	AC input logic low	Note 2	VREF - 0.1			V	1
VIH.CA(AC90)	AC input logic high	-	-	VREF+0.09	Note 2	V	
VIL.CA(AC90)	AC input logic low	-	-	Note 2	VREF - 0.09	V	
VREFCA(DC)	Reference Voltage for ADD, CMD inputs	0.49*VDD	0.51*VDD	0.49*VDD	0.51*VDD	V	2,3

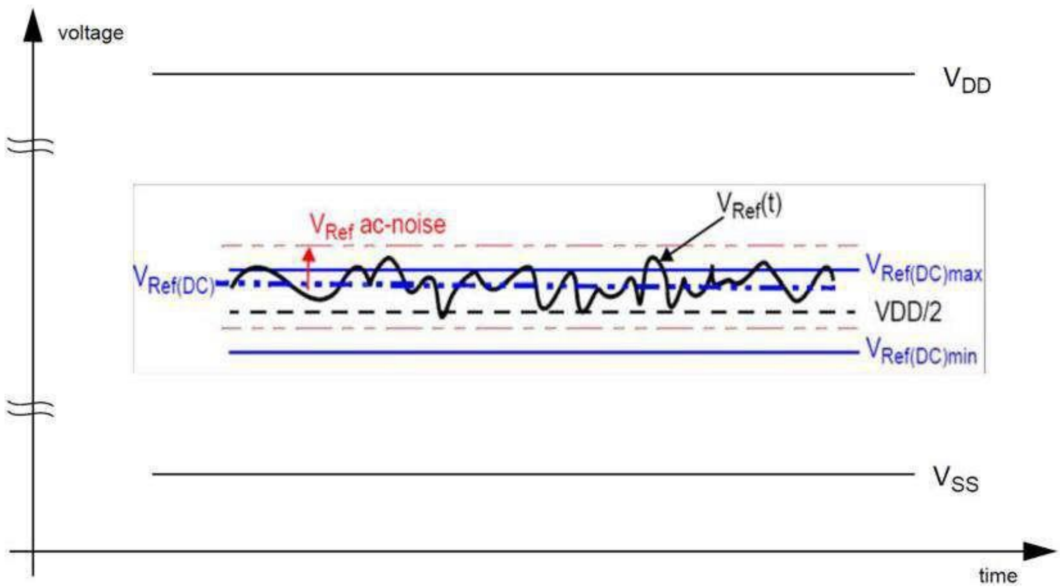
NOTE
1. See “Overshoot and Undershoot Specifications” .
2. The AC peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDD (for reference : approx. ± 12mV) 3. For reference : approx. VDD/2 ± 12mV

VREF Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages VREFCA is illustrated in Illustration of VREF(DC) tolerance and VREF AC-noise limits. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA).

VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Single-ended AC & DC input levels for Command and Address. Furthermore, VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD.

Illustration of VREF(DC) tolerance and VREF AC-noise limits



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF. "VREF" shall be understood as VREF(DC), as defined in Illustration of V.

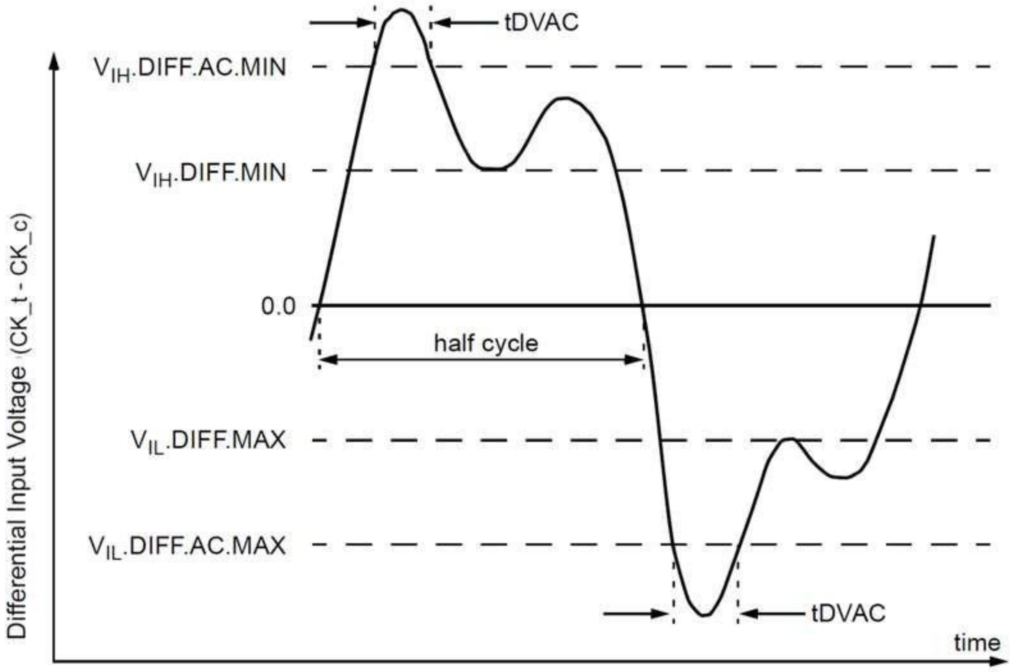
This clarifies, that DC-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VREF(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition

Definition of differential ac-swing and "time above ac-level" tDVAC



Differential swing requirements for clock (CK_t - CK_c)

Differential AC and DC Input Levels

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666		Unit	NOTE
		min	max	min	max		
VIHdiff	Differential input high	+0.150	NOTE 3	+0.135	NOTE 3	V	1
VILdiff	Ddifferential input low	NOTE 3	-0.150	NOTE 3	-0.135	V	1
VIHdiff(AC)	Differential input high (AC)	2 × (VIH(AC) - VREF)	NOTE 3	2 × (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low (AC)	NOTE 3	2 × (VIL(AC) - VREF)	NOTE 3	2 × (VIL(AC) - VREF)	V	2

Symbol	Parameter	DDR4-2933		DDR4-3200		Unit	NOTE
		min	max	min	max		
VIHdiff	Differential input high	+0.125	NOTE 3	+0.110	NOTE 3	V	1
VILdiff	Ddifferential input low	NOTE 3	-0.125	NOTE 3	-0.110	V	1
VIHdiff(AC)	Differential input high (AC)	2 × (VIH(AC) - VREF)	NOTE 3	2 × (VIH(AC) - VREF)	NOTE 3	V	2
VILdiff(AC)	Differential input low (AC)	NOTE 3	2 × (VIL(AC) - VREF)	NOTE 3	2 × (VIL(AC) - VREF)	V	2

NOTE

1. Used to define a differential signal slew-rate.
2. For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.
3. These values are not defined; however, the differential signals (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

Allowed time before ringback (tDVAC) for CK_t - CK_c

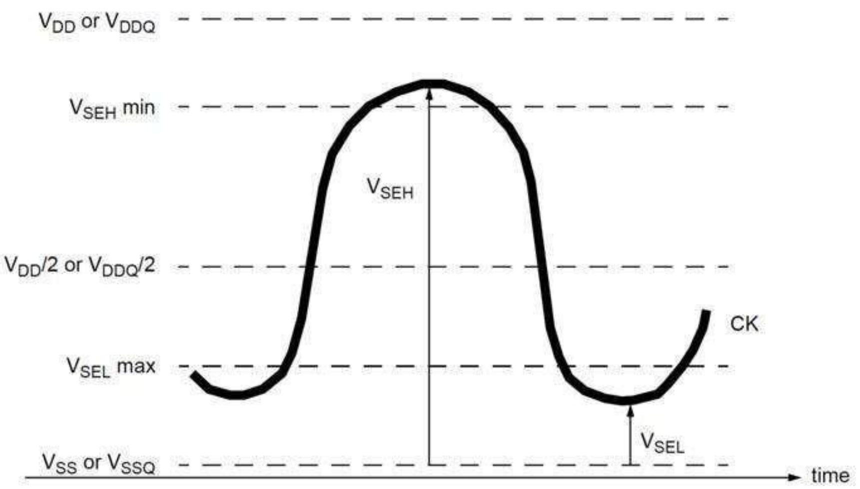
Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(AC)| = 200mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = TBDmV	
	min	max	min	max
> 4.0	120	-	TBD	-
4.0	115	-	TBD	-
3.0	110	-	TBD	-
2.0	105	-	TBD	-
1.8	100	-	TBD	-
1.6	95	-	TBD	-
1.4	90	-	TBD	-
1.2	85	-	TBD	-
1.0	80	-	TBD	-
< 1.0	80	-	TBD	-

Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, CK_c) has to comply with certain requirements for single-ended signals. CK_t and CK_c have to reach approximately VSEHmin/VSEL,max, which are approximately equal to the AC levels VIH(AC) and VIL(AC) for ADD/CMD signals in every half-cycle. The applicable AC levels for ADD/CMD might differ per speed-bin, and so on. For example, if a value other than 100mV is used for ADD/CMD VIH(AC) and VIL(AC) signals, then these AC levels also apply for the singleended signals CK_t and CK_c.

While ADD/CMD signal requirements are with respect to VREFCA, the single-ended components of differential signals have a requirement with respect to VDD/2; this is nominally the same. The transition of single-ended signals through the AC levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL,max/VSEH,min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-Ended Requirements for CK



Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-2133		DDR4-2400/2666		DDR4-2933/3200		Unit	NOTE
		Min	Max	Min	Max	Min	Max		
VSEH	Single-ended high-level for CK_t - CK_c	(VDD/2) +0.100	NOTE3	(VDD/2) +0.095	NOTE3	(VDD/2) +0.085	NOTE3	V	1, 2
VSEL	Single-ended low-level for CK_t - CK_c	NOTE3	(VDD/2) -0.100	NOTE3	(VDD/2) -0.095	NOTE3	(VDD/2) -0.085	V	1, 2

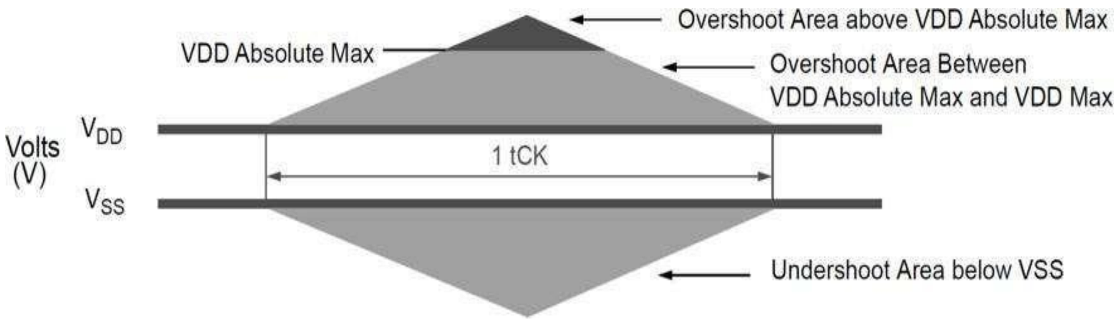
NOTE:
1.For CK_t, CK_c use VIH(AC) and VIL(AC) of ADD/CMD and VREFCA.
2.ADDR/CMD VIH(AC) and VIL(AC) based on VREFCA.
3.These values are not defined; however, the differential signal (CK_t, CK_c) need to be within the respective limits, VIH(DC)max and VIL(DC)min for single-ended signals as well as the limitations for overshoot and undershoot.

Address, Command and Control Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Address, Command and Control pins

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Delta value between VDD Absolute Max and VDD Max allowed for overshoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V-ns
Maximum overshoot area per 1tCK Above Absolute Max	0.0083	0.0071	0.0062	0.0055	0.0055	0.0055	0.0055	V-ns
Maximum overshoot area per 1tCK Between Absolute Max and VDD Max	0.2550	0.2185	0.1914	0.1699	0.1699	0.1699	0.1699	V-ns
Maximum undershoot area per 1tCK Below VSS	0.2644	0.2265	0.1984	0.1762	0.1762	0.1762	0.1762	V-ns
(A0-A13,BG0-BG1,BA0-BA1,ACT_n,RAS_n,CAS_n/A15,WE_n/A14,CS_n,CKE,ODT,C2-C0)								

Address, Command and Control Overshoot and Undershoot Definition

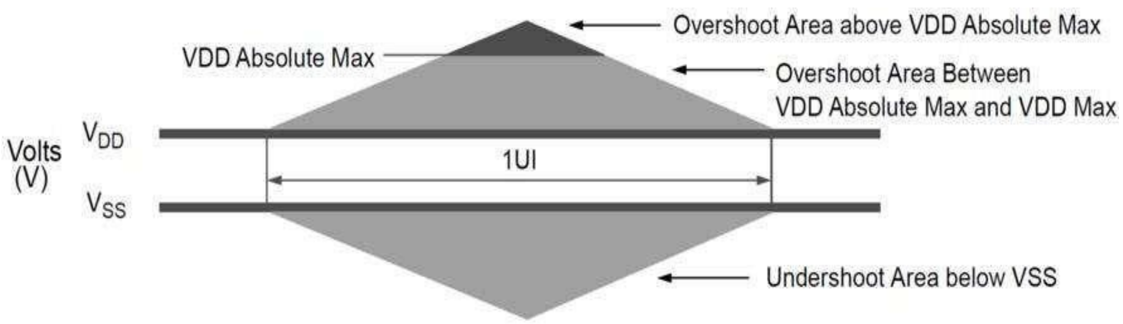


Clock Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Clock

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above VDD Absolute Max allowed for overshoot area	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Delta value between VDD Absolute Max and VDD Max allowed for over-shoot area	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V-ns
Maximum overshoot area per 1UI Above Absolute Max	0.0038	0.0032	0.0028	0.0025	0.0025	0.0025	0.0025	V-ns
Maximum overshoot area per 1UI Between Absolute Max and VDD Max	0.1125	0.0964	0.0844	0.0750	0.0750	0.0750	0.0750	V-ns
Maximum undershoot area per 1UI Below VSS	0.1144	0.0980	0.0858	0.0762	0.0762	0.0762	0.0762	V-ns
(CK_t, CK_c)								

Clock Overshoot and Undershoot Definition

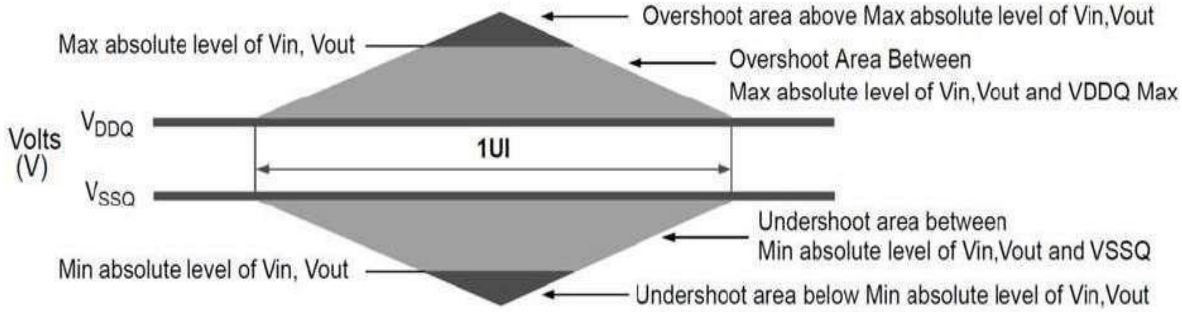


Data, Strobe and Mask Overshoot and Undershoot Specifications

AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification							Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	
Maximum peak amplitude above Max absolute level of Vin, Vout	0.06	0.06	0.06	0.06	0.06	0.06	0.06	V
Overshoot area Between Max Absolute level of Vin, Vout and VDDQ Max	0.24	0.24	0.24	0.24	0.24	0.24	0.24	V
Undershoot area Between Min absolute level of Vin, Vout and VSSQ	0.3	0.3	0.3	0.3	0.3	0.3	0.3	V
Maximum peak amplitude below Min absolute level of Vin, Vout	0.10	0.10	0.10	0.10	0.10	0.10	0.10	V
Maximum overshoot area per 1UI Above Max absolute level of Vin, Vout	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns
Maximum overshoot area per 1UI Between Max absolute level of Vin,Vout and VDDQ Max	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns
Maximum undershoot area per 1UI Between Min absolute level of Vin,Vout and VSSQ	0.1050	0.0900	0.0788	0.0700	0.0700	0.0700	0.0700	V-ns
Maximum undershoot area per 1UI Below Min absolute level of Vin,Vout	0.0150	0.0129	0.0113	0.0100	0.0100	0.0100	0.0100	V-ns
DQS_t, DQS_n, LDQS_t, LDQS_n, UDQS_t, UDQS_n, DQ[0:15], DM/DBI, UDM/UDBI, LDM/LDBI								

Data, Strobe and Mask Overshoot and Undershoot Definition



Slew Rate Definitions

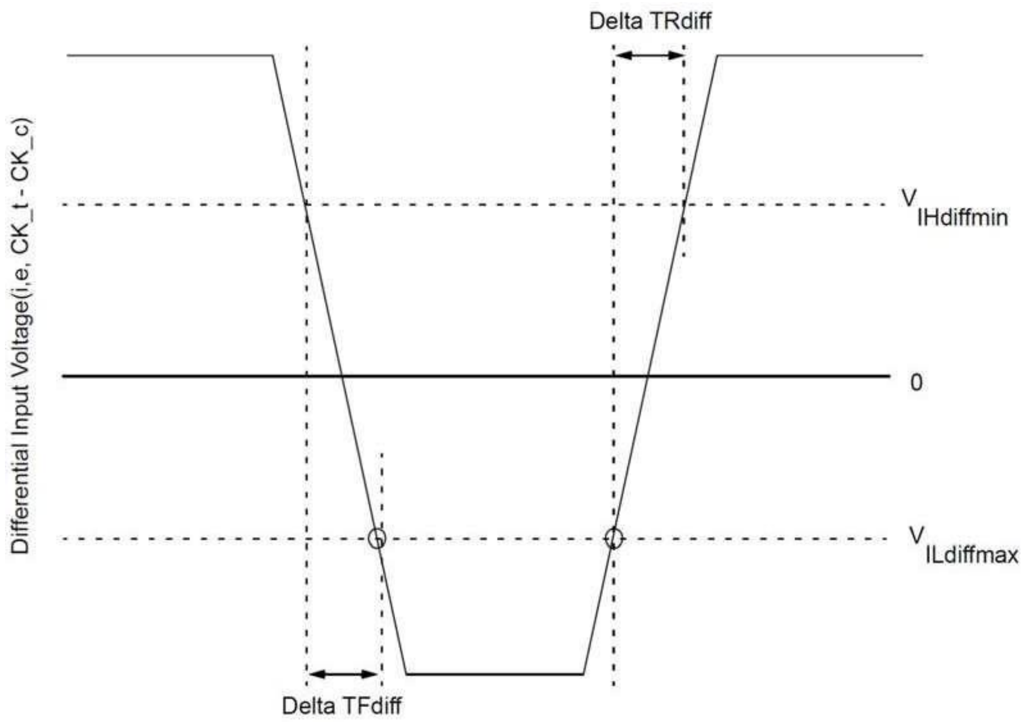
Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table & Figure below.

Differential input slew rate definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	VILdiffmax	VIHdiffmin	[VIHdiffmin – VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			

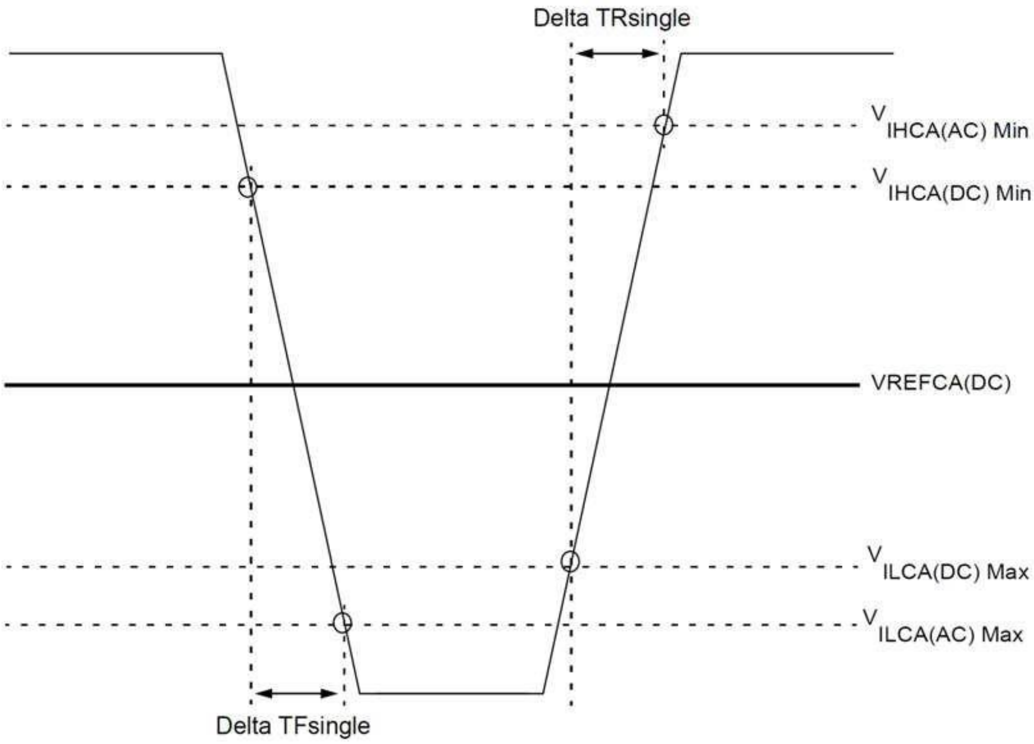
Differential Input Slew Rate Definition for CK_t, CK_c



1.

Slew Rate Definition for Single-ended Input Signals (CMD/ADD)

Single-ended Input Slew Rate definition for CMD and ADD



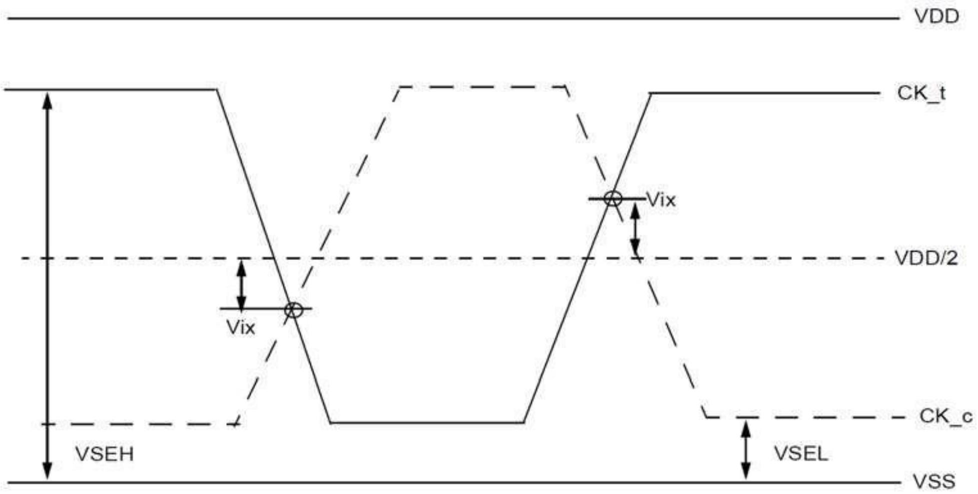
NOTE

1. Single-ended input slew rate for rising edge = { VIHCA(AC)Min - VILCA(DC)Max } / Delta TR single.
2. Single-ended input slew rate for falling edge = { VIHCA(DC)Min - VILCA(AC)Max } / Delta TF single.
3. Single-ended signal rising edge from VILCA(DC)Max to VIHCA(DC)Min must be monotonic slope.
4. Single-ended signal falling edge from VIHCA(DC)Min to VILCA(DC)Max must be monotonic slope.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

Vix Definition (CK)



Cross point voltage for differential input signals (CK)

Symbol	Parameter	Area of VSEH, VSEL	DDR4-1600/1866/2133/2400	
			min	max
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VSEL =< VDD/2 - 145mV	-120	N/A
		VDD/2 - 145mV =< VSEL =< VDD/2 - 100mV	–(VDD/2-VSEL) +25mV	N/A
		VDD/2 + 100mV =< VSEH =< VDD/ 2 + 145mV	N/A	(VSEH - VDD/2) - -25mV
		VDD/2 + 145mV =< VSEH	N/A	120

Symbol	Parameter	Area of VSEH, VSEL	DDR4-2666/2933/3200	
			min	max
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	VSEL =< VDD/2 - 145mV	-110	N/A
		VDD/2 - 145mV =< VSEL =< VDD/2 - 90mV	–(VDD/2-VSEL) +30mV	N/A
		VDD/2 + 100mV =< VSEH =< VDD/ 2 + 145mV	N/A	(VSEH - VDD/2) -30mV
		VDD/2 + 145mV =< VSEH	N/A	110

CMOS rail to rail Input Levels

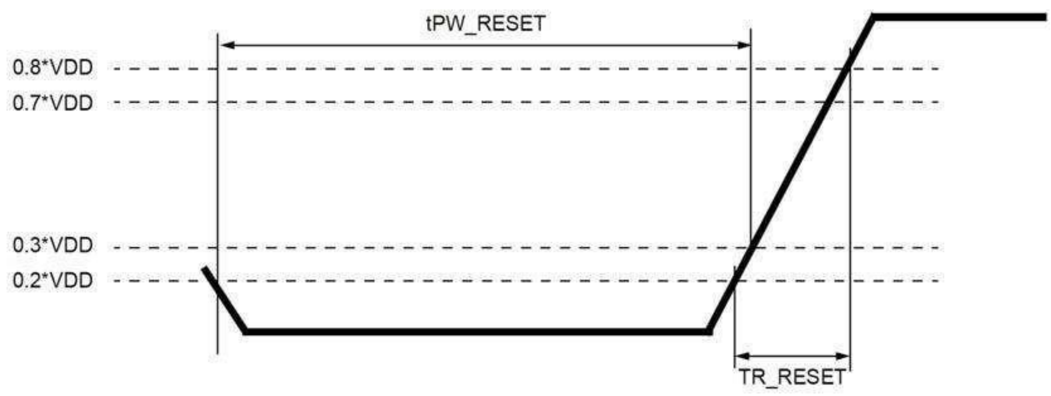
CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :

1. After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings.

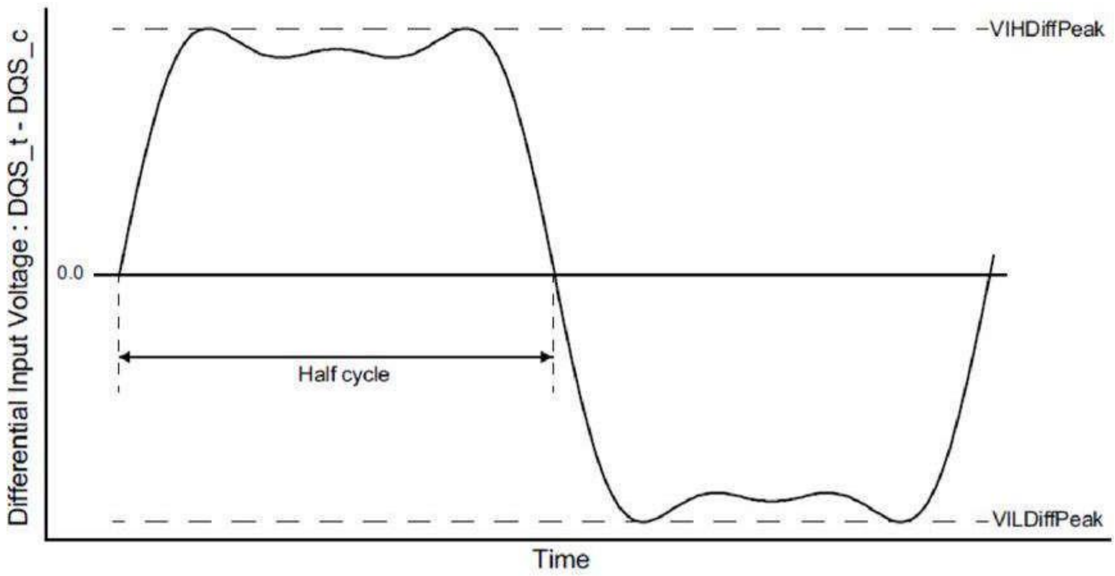
RESET_n Input Slew Rate Definition



AC and DC Logic Input Levels for DQS Signals

Differential signal definition

Definition of differential DQS Signal AC-swing Level



Differential swing requirements for DQS (DQS_t - DQS_c)

Differential AC and DC Input Levels for DQS

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	Note
		min	max	min	max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	186	VDDQ	160	VDDQ	mV	1,2
VILDiffPeak	VIL.DIFF.Peak Voltage	VSSQ	-186	VSSQ	-160	mV	1,2

Symbol	Parameter	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max		
VIHDiffPeak	VIH.DIFF.Peak Voltage	150	VDDQ	150	VDDQ	140	VDDQ	mV	1,2
VILDiffPeak	VIL.DIFF.Peak Voltage	VSSQ	-150	VSSQ	-150	VSSQ	-140	mV	1,2

NOTE

1. Minimum and maximum limits are relative to single-ended portion and can be exceeded within allowed overshoot and undershoot limits.
2. Minimum value point is used to determine differential signal slew-rate.

Peak voltage calculation method

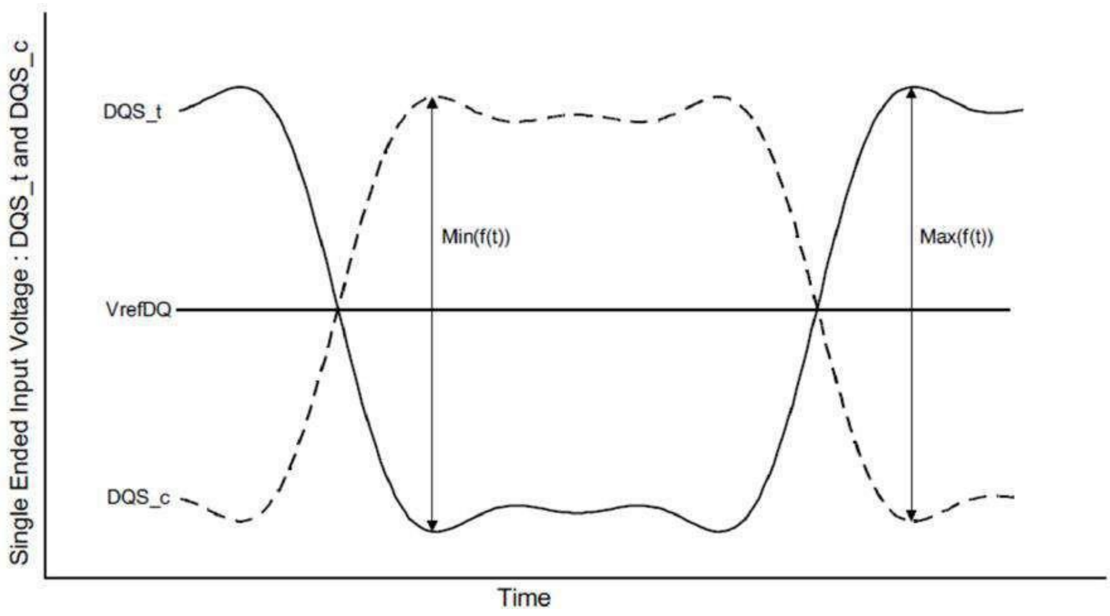
The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t)) VIL.

DIFF.Peak Voltage = Min(f(t))

f(t) = VDQS_t - VDQS_c

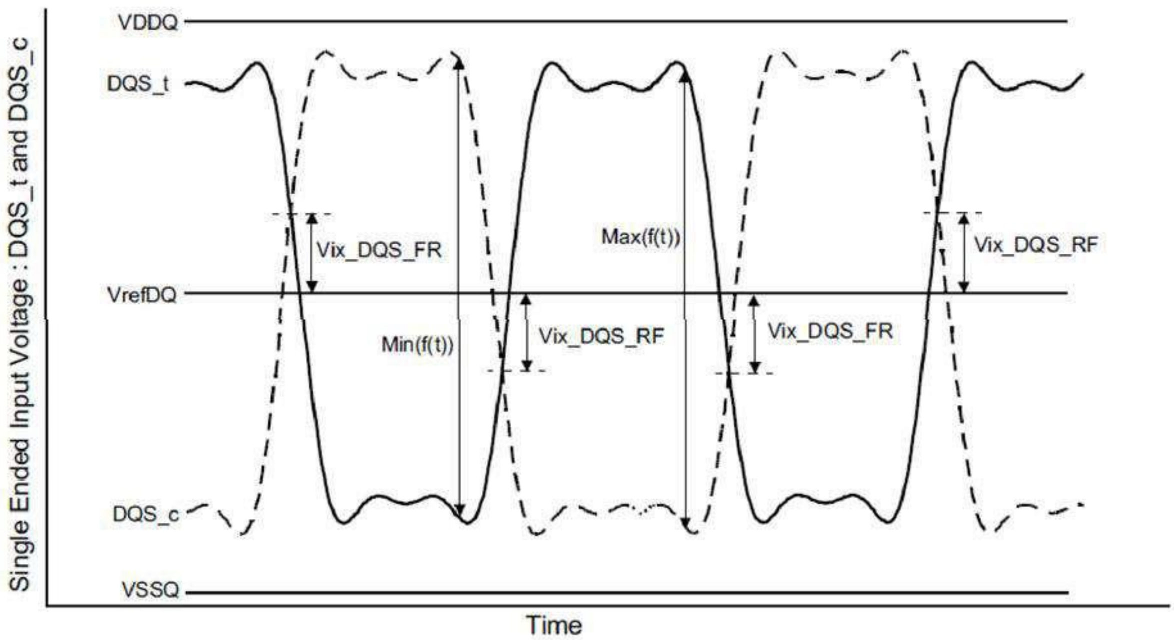
Definition of differential DQS Peak Voltage



Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to strobe, the cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Ta ble 18. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VrefDQ.Vix Definition (DQS)

Vix Definition (DQS)



Cross point voltage for differential input signals (DQS)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200		Unit	Note
		min	max		
VIX_DQS,ratio	DQS Differential input crosspoint voltage ratio	-	25	%	1,2,3

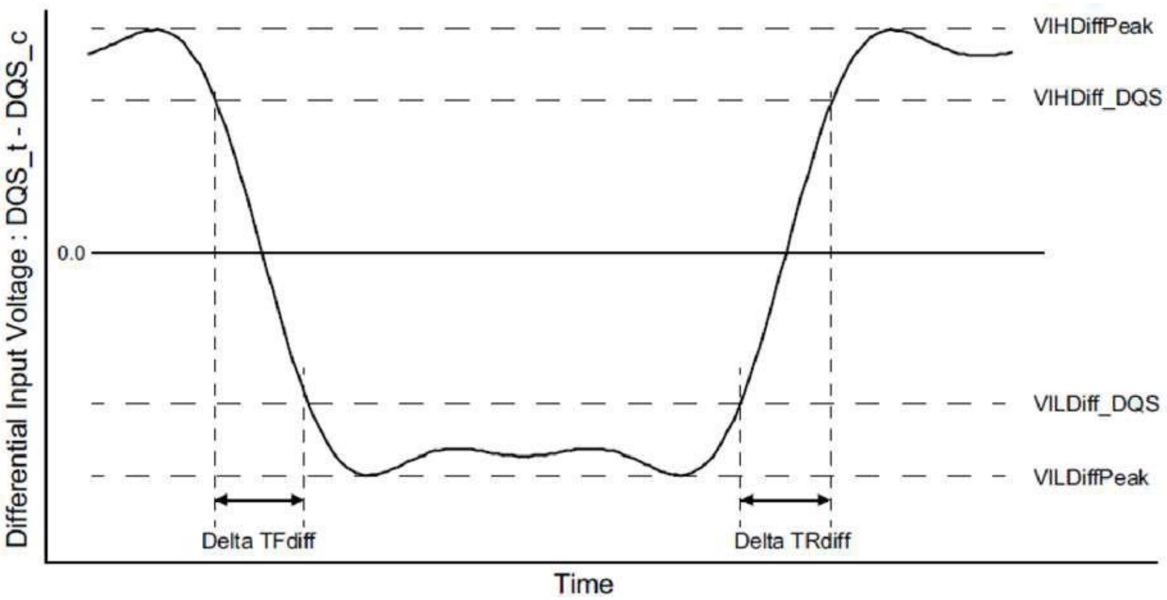
NOTE :

1. The base level of Vix_DQS_FR/RF is VrefDQ that is DDR4 SDRAM internal setting value by Vref Training.
2. Vix_DQS_FR is defined by this equation : Vix_DQS_FR = |Min(f(t)) x Vix_DQS_Ratio.
3. Vix_DQS_RF is defined by this equation : Vix_DQS_RF = Max(f(t)) x Vix_DQS_Ratio.

Differential Input Slew Rate Definition

Input slew rate for diff erential signals (DQS_t, DQS_c) are defined and measured as shown in Figures below.

Differential Input Slew Rate Definition for DQS_t, DQS_c



NOTE

1. Differential signal rising edge from VILDiff_DQS to VIHDiff_DQS must be monotonic slope. 2. Differential signal falling edge from VIHDiff_DQS to VILDiff_DQS must be monotonic slope.

Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILDiff_DQS	VIHDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHDiff_DQS	VILDiff_DQS	|VILDiff_DQS - VIHDiff_DQS|/DeltaTFdiff

Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400		Unit	Note
		min	max	min	max		
VIHDiff_DQS	Differntial Input High	136	-	130	-	mV	1,2
VILDiff_DQS	Differntial Input Low	-	-136	-	-130	mV	1,2

Differential Input Level for DQS_t, DQS_c

Symbol	Parameter	DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max		
VIHDiff_DQS	Differntial Input High	130	-	115	-	110	-	mV	1,2
VILDiff_DQS	Differntial Input Low	-	-130	-	-115	-	-110	mV	1,2

NOTE
1. Differential signal rising edge from VIL,diff,DQS to VIH,diff,DQS must be monotonic slope.
2. Differential signal falling edge from VIH,diff,DQS to VIL,diff,DQS must be monotonic slope.

Differential Input Slew Rate for DQS_t, DQS_c

Symbol	Parameter	DDR4-1600/1866/2133/2400		DDR4-2666/2933/3200		Unit	Note
		min	max	min	max		
SRIdiff	Differential Intput Slew Rate	3	18	2.5	18	V/ns	

AC and DC output Measurement levels

Output Driver DC Electrical Characteristics

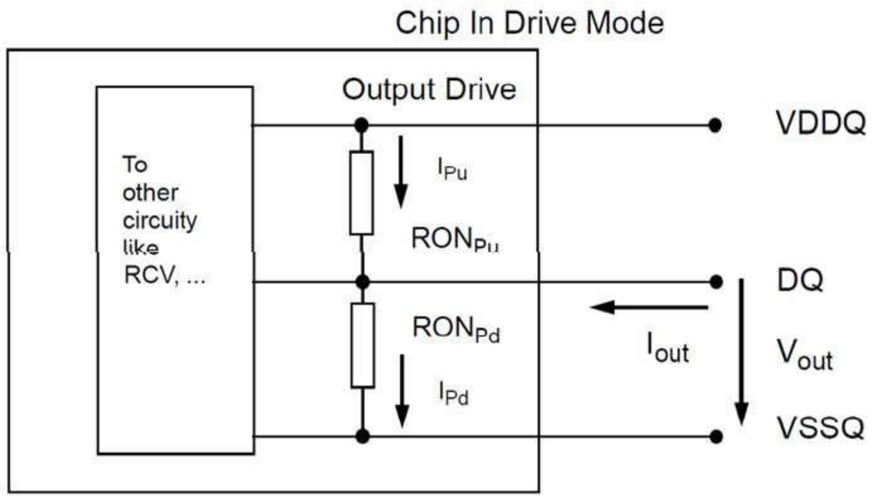
The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I out|}$$ under the condition that RONPd is off

$$RON_{Pd} = \frac{Vout}{|I out|}$$ under the condition that RONPu is off

Output driver



Output Driver DC Electrical Characteristics, assuming RZQ=240ohm; entire operating temperature range; after proper ZQ calibration

RONNOM	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/7	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.73	1	1.1	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.83	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.83	1	1.25	RZQ/5	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	-10	-	17	%	1,2,3,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	-	-	10	%	1,2,4

NOTE

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after cal-ibration, see following section on voltage and temperature sensitivity.
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.
3. 3. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value.

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} *100$$

4. RON variance range ratio to RON Nominal value in a given component, including DQS_t and DQS_c.

$$MMPudd = \frac{RONPuMax - RONPuMin}{RONNOM} *100$$

$$MMPddd = \frac{RONPdMax - RONPdMin}{RONNOM} *100$$

5. This parameter of x16 device is specified for Uper byte and Lower byte.

Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the equations and tables below.

ΔT = T - T(@calibration); ΔV = VDDQ - VDDQ(@ calibration); VDD = VDDQ

Output Driver Sensitivity Definitions

Symbol	Min	Max	Unit
RONPU@ VOH(DC)	0.6 - dRONdTH × |ΔT| - dRONdVH × |ΔV|	1.1 _ dRONdTH × |ΔT| + dRONdVH × |ΔV|	RZQ/6
RON@ VOM(DC)	0.9 - dRONdTM × |ΔT| - dRONdVM × |ΔV|	1.1 + dRONdTM × |ΔT| + dRONdVM × |ΔV|	RZQ/6
RONPD@ VOL(DC)	0.6 - dRONdTL × |ΔT| - dRONdVL × |ΔV|	1.1 + dRONdTL × |ΔT| + dRONdVL × |ΔV|	RZQ/6

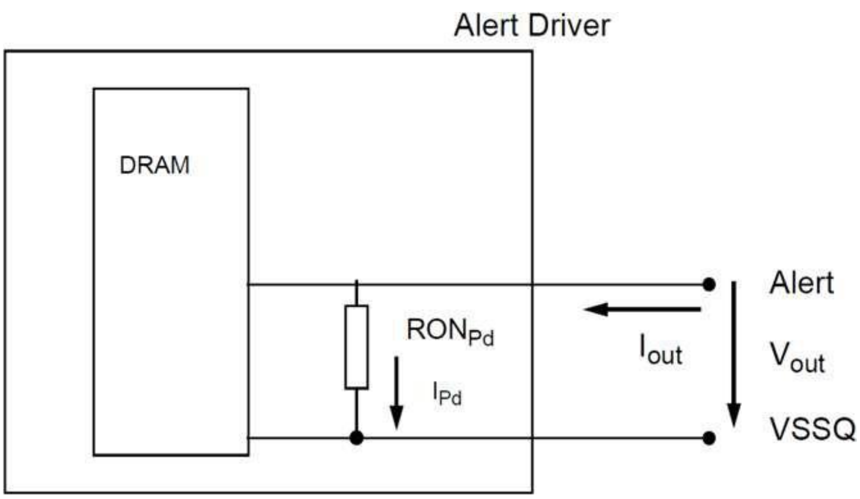
Output Driver Voltage and Temperature Sensitivity

Symbol	Voltage and Temperature Range		Unit
	Min	Max	
dRONdTM	0	1.5	%/°C
dRONdVM	0	0.15	%/mV
dRONdTL	0	1.5	%/°C
dRONdVL	0	0.15	%/mV
dRONdTH	0	1.5	%/°C
dRONdVM	0	0.15	%/mV

Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |} \text{ under the condition that } RON_{Pu} \text{ is off}$$



Resistor	Vout	Min	Max	Unit	NOTE
RONPd	VOLdc= 0.1* VDDQ	0.3	1.2	34Ω	1
	VOMdc = 0.8* VDDQ	0.4	1.2	34Ω	1
	VOHdc = 1.1* VDDQ	0.4	1.4	34Ω	1

Note: 1. VDDQ voltage is at VDDQ(DC).

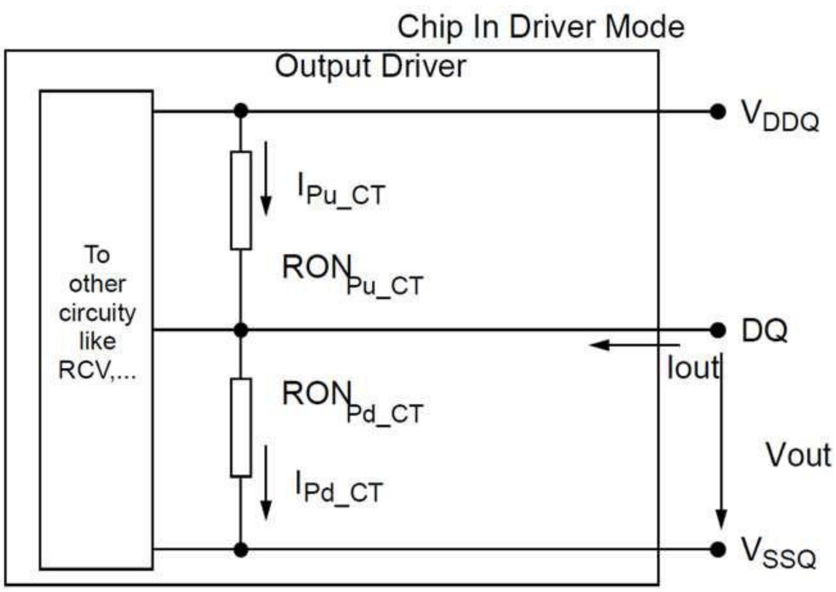
Output Driver Characteristic of Connectivity Test (CT) Mode

Following Output driver impedance RON will be applied Test Output Pin during Connectivity Test (CT) Mode.
The individual pull-up and pull-down resistors (RONPu_CT and RONPd_CT) are defined as follows:

$$RON_{Pu\_CT} = \frac{V_{DDQ} - V_{OUT}}{| Iout |}$$

$$RON_{Pd\_CT} = \frac{V_{OUT}}{| Iout |}$$

Output Driver



RONNOM_CT	Resistor	Vout	Max	Unit	NOTE
34Ω	RONPd_CT	VOBdc = 0.2 x VDDQ	1.9	34Ω	1
		VOLdc = 0.5 x VDDQ	2.0	34Ω	1
		VOMdc = 0.8 x VDDQ	2.2	34Ω	1
		VOHdc = 1.1 x VDDQ	2.5	34Ω	1
	RONPu_CT	VOBdc = 0.2 x VDDQ	2.5	34Ω	1
		VOLdc = 0.5 x VDDQ	2.2	34Ω	1
		VOMdc = 0.8 x VDDQ	2.0	34Ω	1
		VOHdc = 1.1 x VDDQ	1.9	34Ω	1

NOTE : 1. Connectivity test mode uses un-calibrated drivers, showing the full range over PVT. No mismatch between pull up and pull down is defined.

Single-ended AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Unit	NOTE
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1

NOTE

1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Differential AC & DC Output Levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/2933/3200	Unit	NOTE
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	1
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	1

NOTE

1. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ at each of the differential outputs.

Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown below.

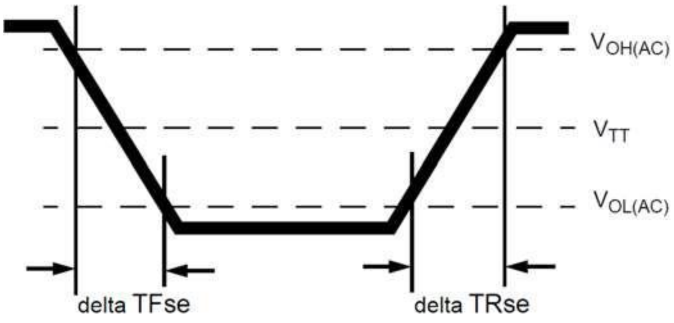
Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC)-VOL(AC)] / Delta TRse
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC)-VOL(AC)] / Delta TFse

NOTE

1. Output slew rate is verified by design and characterization, and may not be subject to production test.

Single-ended Output Slew Rate Definition



Single-ended output slew rate

Parameter	Symbol	DDR4-1600/1866/2133/2400		DDR4-2666		DDR4-2933/3200		Units
		Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	V/ns

Description: SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

NOTE :

1. In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
   - Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
   - Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies.

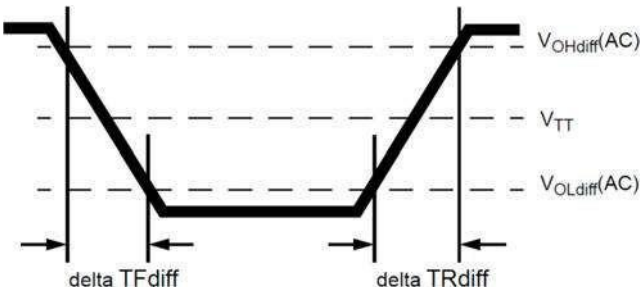
Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table & Figure below.

Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC)-VOLdiff(AC)] / Delta TFdiff

NOTE : 1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential output slew rate

Parameter	Symbol	DDR4-1600/1866/2133/2400		DDR4-2666		DDR4-2933/3200		Units
		Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	V/ns

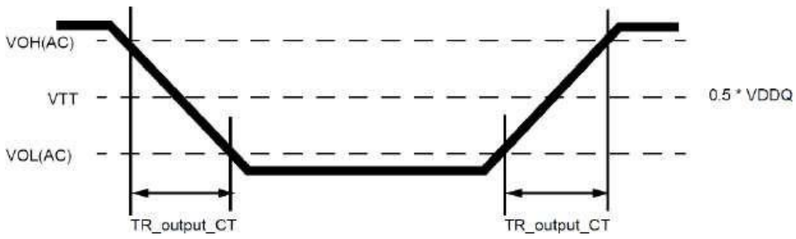
Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

Single-ended AC & DC Output Levels of Connectivity Test Mode

Following output parameters will be applied for DDR4 SDRAM Output Signal during Connectivity Test Mode.

Symbol	Parameter	DDR4-1600 to DDR4-3200	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOB(DC)	DC output below measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + (0.1 x VDDQ)	V	1
VOL(AC)	AC output below measurement level (for output SR)	VTT - (0.1 x VDDQ)	V	1

NOTE 1. The effective test load is 50Ω terminated by VTT = 0.5 * VDDQ.



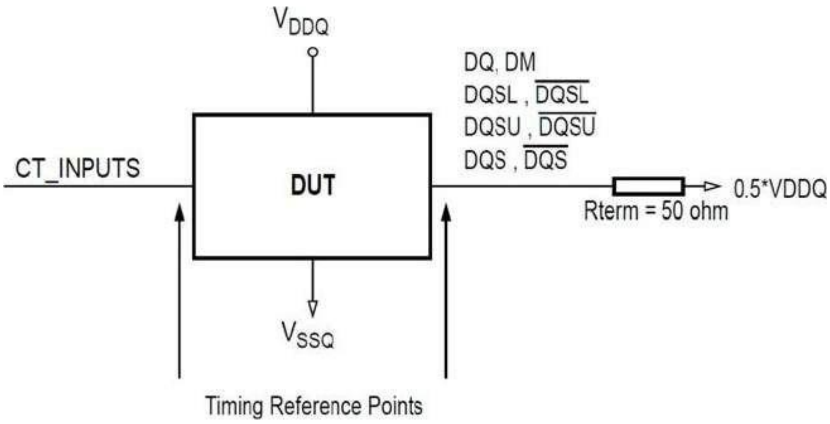
Single-ended output slew rate of Connectivity Test Mode

Parameter	Symbol	DDR4-1600/1866/2133/2400		DDR4-2666		DDR4-2933/3200		Unit
		Min	Max	Min	Max	Min	Max	
Output signal Falling time	TF_output_CT	-	10	-	10	-	10	ns/V
Output signal Rising time	TR_output_CT	-	10	-	10	-	10	ns/V

Test Load for Connectivity Test Mode Timing

The reference load for ODT timings is defined in Figure below.

Connectivity Test Mode Timing Reference Load



Speed Bin

DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600		Unit	NOTE
CL-nRCD-nRP				11-11-11			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75 [12] (13.50) [5,10]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+2nCK	tAA(max)+2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75 [12] (13.50) [5,10]	-	ns	12
PRE command period			tRP	13.75 [12] (13.50) [5,10]	-	ns	12
ACT to PRE command period			tRAS	35	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	48.75 (48.50) [5,10]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) [5,10]	1.6	ns	1,2,3,4,11, 15
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3
Supported CL Settings				9,11,12		nCK	12,14
Supported CL Settings with read DBI				11,13,14		nCK	14
Supported CWL Settings				9,11		nCK	

DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866		Unit	NOTE
CL-nRCD-nRP				13-13-13			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.92 [12] (13.50) [5,10]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+2nCK	tAA(max)+2nCK	ns	12
ACT to internal read or write delay time			tRCD	13.92 [12] (13.50) [5,10]	-	ns	12
PRE command period			tRP	13.92 [12] (13.50) [5,10]	-	ns	12
ACT to PRE command period			tRAS	34	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.92 (47.50) [5,10]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) [5,10]	1.6	ns	1,2,3,4,11,14
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25 (Optional) [5,10]	<1.5	ns	1,2,3,4,6
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved			1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25		1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25		1,2,3
Supported CL Settings				9,11,12,13,14		nCK	12,14
Supported CL Settings with read DBI				11,13,14,15,16		nCK	14
Supported CWL Settings				9,10,11,12		nCK	

DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133		Unit	NOTE
CL-nRCD-nRP				15-15-15			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.06 [12] (13.75) [5,10]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+3nCK	tAA(max)+3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.06 [12] (13.75) [5,10]	-	ns	12
PRE command period			tRP	14.06 [12] (13.75) [5,10]	-	ns	12
ACT to PRE command period			tRAS	33	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	47.06 (46.75) [5,10]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	1.5 (Optional) [5,10]	1.6	ns	1,2,3,4,11,13
	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,7
				(Optional) [5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,7
				(Optional) [5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3
Supported CL Settings				9,11,12,13,14,15,16		nCK	13,14
Supported CL Settings with read DBI				11,13,14,15,16,18,19		nCK	
Supported CWL Settings				9,10,11,12,14		nCK	

DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400		Unit	NOTE
CL-nRCD-nRP				17-17-17			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.16 (13.75) [5,10]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+3nCK	tAA(max)+3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.16 (13.75) [5,10]	-	ns	12
PRE command period			tRP	14.16 (13.75) [5,10]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.16 (45.75) [5,10]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,8
				(Optional) [5,10]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
				(Optional) [5,10]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,8
				(Optional) [5,10]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,8
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21		nCK	
Supported CWL Settings				9,10,11,12,14,16		nCK	

DDR4-2666 Speed Bins and Operations

Speed Bin				DDR4-2666		Unit	NOTE
CL-nRCD-nRP				19-19-19			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	14.25 (13.75) [5,11]	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+3nCK	tAA(max)+3nCK	ns	12
ACT to internal read or write delay time			tRCD	14.25 (13.75) [5,11]	-	ns	12
PRE command period			tRP	14.25 (13.75) [5,11]	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	46.25 (45.75) [5,11]	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,12
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,12
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,9
				(Optional) [5,11]			
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,9
				(Optional) [5,11]			
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,9
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,9
				(Optional) [5,11]			
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,9
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,9
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,9
				(Optional) [5,11]			
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23		nCK	
Supported CWL Settings				9,10,11,12,14,16,18		nCK	

DDR4-2933 Speed Bins and Operations

Speed Bin				DDR4-2933		Unit	NOTE
CL-nRCD-nRP				20-20-20			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.64	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+4nCK	tAA(max)+4nCK	ns	12
ACT to internal read or write delay time			tRCD	13.64	-	ns	12
PRE command period			tRP	13.64	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.64	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,13
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,9
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,15
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,15
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,15
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,15
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,15
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,15
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,15
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,15
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,15
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,15
CWL = 16,20	CL = 19	CL = 23	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 20	CL = 24	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 21	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,21,22		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,24,25,26		nCK	
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

DDR4-3200 Speed Bins and Operations

Speed Bin				DDR4-3200		Unit	NOTE
CL-nRCD-nRP				22-22-22			
Parameter			Symbol	min	max		
Internal read command to first data			tAA	13.75	18.00	ns	12
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min)+4nCK	tAA(max)+4nCK	ns	12
ACT to internal read or write delay time			tRCD	13.75	-	ns	12
PRE command period			tRP	13.75	-	ns	12
ACT to PRE command period			tRAS	32	9 x tREFI	ns	12
ACT to ACT or REF command period			tRC	45.75	-	ns	12
	Normal	Read DBI					
CWL = 9	CL = 9	CL = 11	tCK(AVG)	Reserved		ns	1,2,3,4,11
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	ns	1,2,3,4,10
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	ns	1,2,3,10
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	ns	1,2,3,4,10
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	ns	1,2,3,10
CWL = 11,14	CL = 14	CL = 17	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 15	CL = 18	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
	CL = 16	CL = 19	tCK(AVG)	0.937	<1.071	ns	1,2,3,4,10
CWL = 12,16	CL = 15	CL = 18	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 16	CL = 19	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 17	CL = 20	tCK(AVG)	0.833	<0.937	ns	1,2,3,4,10
	CL = 18	CL = 21	tCK(AVG)	0.833	<0.937	ns	1,2,3,10
CWL = 14,18	CL = 17	CL = 20	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 18	CL = 21	tCK(AVG)	Reserved		ns	1,2,3,4,10
	CL = 19	CL = 22	tCK(AVG)	0.75	<0.833	ns	1,2,3,4,10
	CL = 20	CL = 23	tCK(AVG)	0.75	<0.833	ns	1,2,3,10
CWL = 16,20	CL = 20	CL = 24	tCK(AVG)	Reserved		ns	1,2,3,4
	CL = 22	CL = 26	tCK(AVG)	0.682	<0.75	ns	1,2,3,4
	CL = 24	CL = 28	tCK(AVG)	0.682	<0.75	ns	1,2,3
Supported CL Settings				10,11,12,13,14,15,16,17,18,19,20,22,24		nCK	13
Supported CL Settings with read DBI				12,13,14,15,16,18,19,20,21,22,23,24,26,28		nCK	
Supported CWL Settings				9,10,11,12,14,16,18,20		nCK	

Speed Bin Table Note

Absolute Specification

- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133, 2400, 2666, 2933 and 3200 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
9. Any DDR4-2666 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
10. Any DDR4-2933/3200 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
11. 10 DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).
15. Each speed bin lists the timing requirements that need to be supported in order for a given DRAM to be JEDEC compliant. JEDEC compliance does not require support for all speed bins within a given speed. JEDEC compliance requires meeting the parameters for a least one of the listed speed bins.

IDD and IDDQ Specification Parameters and Test conditions

IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. F igure below shows the setup and test load for IDD, IPP and IDDQ measurements.

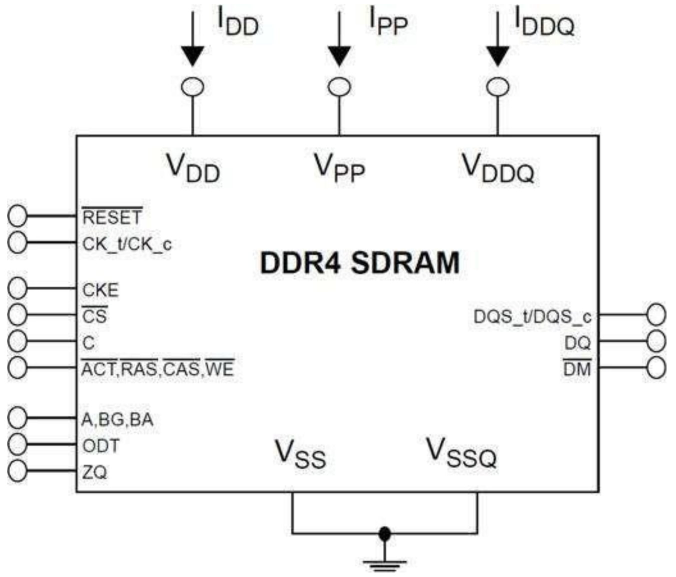
- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 22. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 36.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 37.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 38 through Table 46.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  - RON = RZQ/7 (34 Ohm in MR1);
  - RTT_NOM = RZQ/6 (40 Ohm in MR1);
  - RTT_WR = RZQ/2 (120 Ohm in MR2);
  - RTT_PARK = Disable;
  - Qoff = 0B (Output Buffer enabled) in MR1;
  - TDQS_t disabled in MR1;
  - CRC disabled in MR2;
  - CA parity feature disabled in MR5;
  - Gear down mode disabled in MR3;
  - Read/Write DBI disabled in MR5;
  - DM disabled in MR5

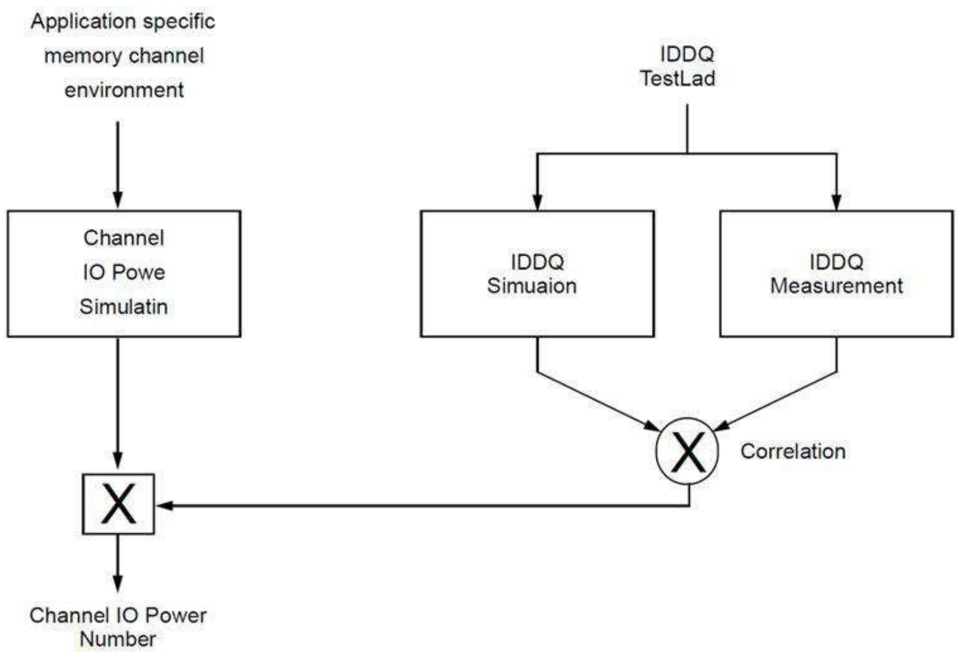
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, LOW, LOW, LOW, LOW} ; apply BG/BA changes when directed.
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH} apply invert of BG/BA changes when directed above.

Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements



NOTE: 1. DIMM level Output test load condition may be different from above

Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement



Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400			DDR4-2666			DDR4-2933			DDR4-3200			Unit
		10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	15-15-15	16-16-16	18-18-18	17-17-17	18-18-18	19-19-19	20-20-20	21-21-21	22-22-22	23-23-23	24-24-24	25-25-25	
tCK		1.25			1.071			0.938			0.833			0.75			0.685			0.625			ns
CL		10	11	12	12	13	14	14	15	16	15	16	18	17	18	19	20	21	22	20	22	24	CK
CWL		9	11	11	10	12	12	11	14	14	12	16	16	14	18	18	14	18	18	16	20	20	CK
nRCD		10	11	12	12	13	14	14	15	16	15	16	18	17	18	19	20	21	22	20	22	24	CK
nRC		38	39	40	44	45	46	50	51	52	54	55	57	60	61	62	66	67	68	72	74	76	CK
nRAS		28			32			36			39			43			47			52			CK
nRP		10	11	12	12	13	14	14	15	16	15	16	18	17	18	19	20	21	22	20	22	24	CK
nFAW	x4	16			16			16			16			16			16			16			CK
	x8	20			22			23			26			28			31			34			CK
	x16	28			28			32			36			40			44			48			CK
nRRDS	x4	4			4			4			4			4			4			4			CK
	x8	4			4			4			4			4			4			4			CK
	x16	5			5			6			7			7			8			9			CK
nRRDL	x4	5			5			6			6			7			8			8			CK
	x8	5			5			6			6			7			8			8			CK
	x16	6			6			7			8			9			10			11			CK
tCCD_S		4			4			4			4			4			4			4			CK
tCCD_L		5			5			6			6			7			8			8			CK
tWTR_S		2			3			3			3			4			4			4			CK
tWTR_L		6			7			8			9			10			11			12			CK
nREFI		6,240			7,283			8,324			9,364			10,400			11,437			12,480			CK
nRFC 2Gb		128			150			171			193			214			235			256			CK
nRFC 4Gb		208			243			278			313			347			382			416			CK
nRFC 8Gb		280			327			374			421			467			514			560			CK
nRFC 16Gb		440			514			587			660			734			807			880			CK

NOTE: 1. 1KB based x4 use same numbers of clocks for *n*FAW as the x8.

Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0) CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling (see IDD0, IDD0A and IPP0 Measurement-Loop Pattern); **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD0, IDD0A and IPP0 Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see "IDD0, IDD0A and IPP0 Measurement-Loop Pattern"
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0) CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL** : see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling (see IDD1, IDD1A and IPP1 Measurement-Loop Pattern); **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see IDD1, IDD1A and IPP1 Measurement-Loop Pattern); **Output Buf-fer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see "IDD1, IDD1A and IPP1 Measurement-Loop Pattern"
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0) CKE**: High; **External clock:** On; **tCK, CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling (see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern); **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern
IDD2NA	**Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current CKE**: High; **External clock:** On; **tCK, CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling (see IDD2NT and IDDQ2NT Measurement-Loop Pattern); **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling (see IDD2NT and IDDQ2NT Measurement-Loop Pattern); **Pattern Details:** see (see IDD2NT and IDDQ2NT Measurement-Loop Pattern)
IDDQ2NT (optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled [3,5]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled [3,5]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled [3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled [3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL** : see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current Same condition with IDD2P**

Symbol	Description
IDD2Q	**Precharge Quiet Standby Current CKE**: High; **External clock:** On; **tCK, CL**: see “Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns”; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IDD3N	**Active Standby Current CKE**: High; **External clock:** On; **tCK, CL**: see “Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns”; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling see “IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern”; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see “IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern”
IDD3NA	**Active Standby Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current Same condition with IDD3N**
IDD3P	**Active Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see “Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns”; **BL:** 8 [1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current Same condition with IDD3P**
IDD4R	**Operating Burst Read Current CKE:** High; **External clock:** On; **tCK, CL** : see “Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns”; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to “IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern”; **Data IO:** seamless read data burst with different data between one burst and the next one according to “IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern”; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see “IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern”
IDD4RA	**Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current Same condition with IDD4R**
IDDQ4R (optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current CKE:** High; **External clock:** On; **tCK, CL** : see “Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns”; **BL:** 8 [1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to “IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern”; **Data IO:** seamless write data burst with different data between one burst and the next one according to “IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern”; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern
IDD4WA	**Operating Burst Write Current (AL=CL-1)**
IDD4WB	**Operating Burst Write Current with Write DBI Write DBI enabled[3], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current Same condition with IDD4W**

Symbol	Description
IDD5B	**Burst Refresh Current (1X REF) CKE:** High; **External clock:** On; **tCK, CL, nRFC** : see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to "IDD5B Measurement-Loop Pattern"; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see IDD5B Measurement-Loop Pattern); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see "IDD5B Measurement-Loop Pattern"
IPP5B	**Burst Refresh Write IPP Current (1X REF) Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF) Same condition with IDD5F2**
IDD5F4	**Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF) Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range *T*CASE:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers [2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) ***T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers [2]; **ODT Signal:** MID-LEVEL
IPP6E	**Self Refresh IPP Current: Extended Temperature Range Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range *T*CASE:** 0 - 45°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers [2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current *T*CASE:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto4;**CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL** : see "Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns"; **BL:** 8 [1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to "IDD7 Measurement-Loop Pattern"; **Data IO:** read data bursts with different data between one burst and the next one according to "IDD7 Measurement-Loop Pattern"; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see "IDD7 Measurement-Loop Pattern"; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see "IDD7 Measurement-Loop Pattern"
IPP7	**Operating Bank Interleave Read IPP Current Same condition with IDD7**
IDD8	**Maximum Power Down Current TBD**
IPP8	**Maximum Power Down IPP Current Same condition with IDD8**

NOTE :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable
   - set MR1 [A12 = 0] : Qoff = Output buffer enabled
   - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
   RTT_Nom enable
   - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6
   RTT_WR enable
   - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2
   RTT_PARK disable
   - set MR5 [A8:6 = 000].
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
   010] : 1866MT/s, 2133MT/s
   011] : 2400MT/s
   Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate DLL disabled : set MR1 [A0 = 0]
   CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
   010] : 2400MT/s
   Read DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
   01] : Reduced Temperature range
   10] : Extended Temperature range
   11] : Auto Self Refresh
5. IDD2NG should be measured after sync pulse(NOP) input.

IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[b]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	0	1	**1**	**0**	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	**0**	**0**	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	**0**	3[b]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	**0**	**1**	1	0	0	0	0	**0**	**0**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		8	7*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
		11	11*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
		13	13*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] =** 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 0 instead																

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
2. BG1 is don't care for x16 device
3. C[2:0] are used only for 3DS device 4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**RD**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command.

IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**WR**	0	1	1	0	1	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	1	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**WR**	0	1	1	0	1	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	1	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**WR**	0	1	1	0	1	1	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC**
			1,2	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3,4	D#, D#	1	1	1	1	1	1	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	5	**WR**	0	1	1	0	1	1	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC**
			6,7	D, D	1	0	0	0	0	1	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			8,9	D#, D#	1	1	1	1	1	1	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Write Command.

IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**REF**	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
		1	1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			4	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			4-7	repeat pattern 1...4, use **BG[1:0][2] = 1, BA[1:0] = 1** instead																
			8-11	repeat pattern 1...4, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
			12-15	repeat pattern 1...4, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
			16-19	repeat pattern 1...4, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
			20-23	repeat pattern 1...4, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
			24-27	repeat pattern 1...4, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
			28-31	repeat pattern 1...4, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
			32-35	repeat pattern 1...4, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
			40-43	repeat pattern 1...4, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
			44-47	repeat pattern 1...4, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
			48-51	repeat pattern 1...4, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
			52-55	repeat pattern 1...4, use **BG[1:0][2] = 3, BA[1:0] = 2** instead																
			56-59	repeat pattern 1...4, use **BG[1:0][2] = 2, BA[1:0] = 3** instead																
			60-63	repeat pattern 1...4, use **BG[1:0][2] = 3, BA[1:0] = 0** instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE :

1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. DQ signals are VDDQ.

IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	**RDA**	0	1	1	0	1	0		**0**	**0**	0	0	1	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**	0	-
			nRRD + 1	**RDA**	0	1	1	0	1	0		**1**	**1**	0	0	1	**0**	**0**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**2 **= 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0]**2 **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**2 **= 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 3, BA[1:0] = 3** instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0]**2 **= 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**2 **= 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**2 **= 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE :
1. DQS_t, DQS_c are VDDQ.
2. BG1 is don't care for x16 device.
3. C[2:0] are used only for 3DS device.
4. Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

IDD Specification

IDD and IPP values are for typical operating range of voltage and temperature unless otherwise noted.

Symbol	Width	DDR4-2666	DDR4-3200	Unit
		19-19-19	22-22-22	
IDD0: One bank ACTIVATE-to-RECHARGE current	x4, x8	71	73	mA
	x16	75	82	mA
IPP0: One bank ACTIVATE-to-RECHARGE IPP current	ALL	6	6	mA
IDD1: One bank ACTIVATE-to-READ-to-PRECHARGE current	x4, x8	90	95	mA
	x16	106	111	mA
IDD2N: Precharge standby current	ALL	53	59	mA
IDD2NT: Precharge standby ODT current	ALL	76	79	mA
IDD2P: Precharge powerdown current	ALL	29	29	mA
IDD2Q: Precharge quiet standby current	ALL	39	40	mA
IDD3N: Active standby current	ALL	76	84	mA
IPP3N: Active standby IPP current	ALL	2	2	mA
IDD3P: Active power-down current	ALL	43	45	mA
IDD4R: Burst read current	x4	155	169	mA
	x8	193	198	mA
	x16	268	278	mA
IDD4W: Burst write current	x4	174	182	mA
	x8	202	206	mA
	x16	264	268	mA
IDD5R: Burst refresh current (1X REF)	x4	146	156	mA
	x8	151	157	mA
	x16	156	159	mA
IPP5R: Burst refresh IPP current (1X REF)	ALL	37	37	mA
IDD6N: Self refresh current; 0–85°C [1]	ALL	29	29	mA
IDD6E: Self refresh current; 0–95°C [2]	ALL	32	32	mA
IDD6R: Self refresh current; 0–45C [3, 4]	ALL	25	25	mA
IDD6A: Auto self refresh current	ALL	30	30	mA
IPP6x: Auto self refresh current [23]	ALL	4.1	4.1	mA

Symbol	Width	DDR4-2666	DDR4-3200	Unit
		19-19-19	22-22-22	
IDD7: Bank interleave read current	x4	235	236	mA
	x8	245	247	mA
	x16	275	278	mA
IPP7: Bank interleave read IPP current	x4, x8	50	50	mA
	x16	34	34	mA
IDD8: Maximum powerdown current	ALL	22	22	mA

NOTE
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A7 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A7 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. IDD6R and IDD6A values are typical.
5. When additive latency is enabled for IDD0, current changes by approximately 9%.
6. When additive latency is enabled for IDD1 , current changes by approximately +14% (x4/x8), +14% (x16).
7. When additive latency is enabled for IDD2N , current changes by approximately +0.0%.
8. When DLL is disabled for IDD2N, current changes by approximately 1%.
9. When CAL is enabled for IDD2N, current changes by approximately –34%.
10. When gear-down is enabled for IDD2N, current changes by approximately 0%.
11. When CA parity is enabled for IDD2N, current changes by approximately +15%.
12. When additive latency is enabled for IDD3N, current changes by approximately +9%.
13. When additive latency is enabled for IDD4R, current changes by approximately +6%.
14. When read DBI is enabled for IDD4R, current changes by approximately -8%.
15. When additive latency is enabled for IDD4W, current changes by approximately +6% (x4/8), +4% (x16).
16. When write DBI is enabled for IDD4W, current changes by approximately 13%.
17. When write CRC is enabled for IDD4W, current changes by approximately 4%.
18. When CA parity is enabled for IDD4W, current changes by approximately +15% (x4/x8), +10% (x16).
19. When 2X REF is enabled for IDD5R, current changes by approximately –16%.
20. When 4X REF is enabled for IDD5R, current changes by approximately –35%.
21. IPP0 test and limit is applicable for IDD0 and IDD1 conditions.
22. IPP3N test and limit is applicable for all IDD2x, IDD3x, IDD4x and IDD8 conditions; that is, testing IPP3N should satisfy the IPPs for the noted IDD tests.
23. IPP6x is applicable to IDD6N, IDD6E, IDD6R and IDD6A conditions.

Input/Output Capacitance

Silicon Pad Input/Output Capacitance

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400,2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max	min	max		
CIO	Input/output capacitance	0.55	1.4	0.55	1.15	0.55	1.15	0.55	1.00	pF	1,2,3
CCK	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.7	pF	2,3
CDCK	Input capacitance delta CK_t and CK_c	0	0.05	0	0.05	0	0.05	0	0.05	pF	2,3,6
CDDQS	Input/output capacitance delta	0	0.05	0	0.05	0	0.05	0	0.05	pF	2,3,5
CI	Input capacitance (CTRL, ADD, CMD pins	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.55	pF	2,3,4
CDI_ CTRL	Input capacitance delta (All CTRL pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	2,3,8,9
CDI_ ADD_CMD	Input capacitance delta (All ADD/ CMD pins only)	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,10, 11
CDIO	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	-0.1	0.1	-0.1	0.1	pF	1,2,3,4
CALERT	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	2,3
CZQ	Input/output capacitance of ZQ	-	2.3	-	2.3	-	2.3	-	2.3	pF	2,3,12
CTEN	Input/output capacitance of TEN	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	2,3,13

NOTE

1. Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to a production test; it is verified by design and characterization.
3. The capacitance is measured with VDD, VDDQ, VSS, and VSSQ applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). VDD = VDDQ = 1.5V, VBIAS = VDD/2 and on-die termination off.
4. This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.
5. CDIO = CIO(DQ, DM) - 0.5 × (CIO(DQS_t) + CIO(DQS_c)).
6. Absolute value of CIO (DQS_t), CIO (DQS_c)
7. Absolute value of CCK_t, CCK_c
8. CI applies to ODT, CS_n, CKE, A[17:0], BA[1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
9. CDI_CTRL applies to ODT, CS_n, and CKE.
10. CDI_CTRL = CI(CTRL) - 0.5 × (CI(CLK_t) + CI(CLK_c)).
11. CDI_ADD_CMD applies to A[17:0], BA1:0], BG[1:0], RAS_n, CAS_n, ACT_n, PAR and WE_n.
12. CDI_ADD_CMD = CI(ADD_CMD) - 0.5 × (CI(CLK_t) + CI(CLK_c)).
13. Maximum external load capacitance on ZQ pin: 5pF.
14. Only applicable if TEN pin does not have an internal pull-up.

DRAM package electrical specifications (x4/x8)

Symbol	Parameter	DDR4-1600/1866/2133/2400,2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max		
ZIO	Input/output Zpkg	45	85	48	85	48	85	Ω	1
TdIO	Input/output Pkg Delay	14	42	14	42	14	40	ps	1
Lio	Input/Output Lpkg	-	3.3	-	3.3	-	3.3	nH	1,2
Cio	Input/Output Cpkg	-	0.78	-	0.78	-	0.78	pF	1,3
ZDIO DQS	DQS_t, DQS_c Zpkg	45	85	48	85	48	85	Ω	1
TdDIO DQS	DQS_t, DQS_c Pkg Delay	14	42	14	42	14	40	ps	1
Lio DQS	DQS Lpkg	-	3.3	-	3.3	-	3.3	nH	1,2
Cio DQS	DQS Cpkg	-	0.78	-	0.78	-	0.78	pF	1,3
DZDIO DQS	Delta Zpkg DQSU_t and DQSU_c	-	10	-	10	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	-	10	-	10	Ω	-
DTdDIO DQS	Delta Delay DQSU_t and DQSU_c	-	5	-	5	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	-	5	-	5	ps	-
ZI CTRL	Input- CTRL pins Zpkg	50	90	50	90	50	90	Ω	1
TdI_ CTRL	Input- CTRL pins Pkg Delay	14	42	14	42	14	40	ps	1
Li CTRL	Input CTRL Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Ci CTRL	Input CTRL Cpkg	-	0.7	-	0.7	-	0.7	pF	1,3
ZIADD CMD	Input- CMD ADD pins Zpkg	50	90	50	90	50	90	Ω	1
TdIADD_ CMD	Input- CMD ADD pins Pkg Delay	14	45	14	40	14	40	ps	1
Li ADD CMD	Input CMD ADD Lpkg	-	3.6	-	3.6	-	3.6	nH	1,2
Ci ADD CMD	Input CMD ADD Cpkg	-	0.74	-	0.74	-	0.74	pF	1,3
ZCK	CK_t and CK_c Zpkg	50	90	50	90	50	90	Ω	1
TdCK	CK_t and CK_c Pkg Delay	14	42	14	42	14	42	ps	1
Li CLK	Input CLK Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Ci CLK	Input CLK Cpkg	-	0.7	-	0.7	-	0.7	pF	1,3
DZDCK	Delta Zpkg CK_t and CK_c	-	10	-	10	-	10	Ω	-
DTdCK	Delta Delay CK_t and CK_c	-	5	-	5	-	5	ps	-
ZOZQ	ZQ Zpkg	-	100	-	100	-	100	Ω	-
TdO ZQ	ZQ Delay	20	90	20	90	20	90	ps	-
ZO ALERT	ALERT Zpkg	40	100	40	100	40	100	Ω	-
TdO ALERT	ALERT Delay	20	55	20	55	20	55	ps	-

NOTE

1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td.
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

DRAM package electrical specifications (x16)

Symbol	Parameter	DDR4-1600/1866/2133/2400,2666		DDR4-2933		DDR4-3200		Unit	Note
		min	max	min	max	min	max		
ZIO	Input/output Zpkg	45	85	48	85	48	85	Ω	1
TdIO	Input/output Pkg Delay	14	45	14	45	14	45	ps	1
Lio	Input/Output Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Cio	Input/Output Cpkg	-	0.82	-	0.82	-	0.82	pF	1,3
ZDIO DQS	DQS_t, DQS_c Zpkg	45	85	48	85	48	85	Ω	1
TdDIO DQS	DQS_t, DQS_c Pkg Delay	14	45	14	45	14	45	ps	1
Lio DQS	DQS Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Cio DQS	DQS Cpkg	-	0.82	-	0.82	-	0.82	pF	1,3
DZDIO DQS	Delta Zpkg DQSU_t and DQSU_c	-	10	-	10	-	10	Ω	-
	Delta Zpkg DQSL_t, DQSL_c	-	10	-	10	-	10	Ω	-
DTdDIO DQS	Delta Delay DQSU_t and DQSU_c	-	5	-	5	-	5	ps	-
	Delta Delay DQSL_t, DQSL_c	-	5	-	5	-	5	ps	-
ZI CTRL	Input- CTRL pins Zpkg	50	90	50	90	50	90	Ω	1
TdI_ CTRL	Input- CTRL pins Pkg Delay	14	42	14	42	14	42	ps	1
Li CTRL	Input CTRL Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Ci CTRL	Input CTRL Cpkg	-	0.7	-	0.7	-	0.7	pF	1,3
ZIADD CMD	Input- CMD ADD pins Zpkg	50	90	50	90	50	90	Ω	1
TdIADD_ CMD	Input- CMD ADD pins Pkg Delay	14	52	14	52	14	52	ps	1
Li ADD CMD	Input CMD ADD Lpkg	-	3.9	-	3.9	-	3.9	nH	1,2
Ci ADD CMD	Input CMD ADD Cpkg	-	0.86	-	0.86	-	0.86	pF	1,3
ZCK	CK_t and CK_c Zpkg	50	90	50	90	50	90	Ω	1
TdCK	CK_t and CK_c Pkg Delay	14	42	14	42	14	42	ps	1
Li CLK	Input CLK Lpkg	-	3.4	-	3.4	-	3.4	nH	1,2
Ci CLK	Input CLK Cpkg	-	0.7	-	0.7	-	0.7	pF	1,3
DZDCK	Delta Zpkg CK_t and CK_c	-	10	-	10	-	10	Ω	-
DTdCK	Delta Delay CK_t and CK_c	-	5	-	5	-	5	ps	-
ZOZQ	ZQ Zpkg	-	100	-	100	-	100	Ω	-
TdO ZQ	ZQ Delay	20	90	20	90	20	90	ps	-
ZO ALERT	ALERT Zpkg	40	100	40	100	40	100	Ω	-
TdO ALERT	ALERT Delay	20	55	20	55	20	55	ps	-

NOTE

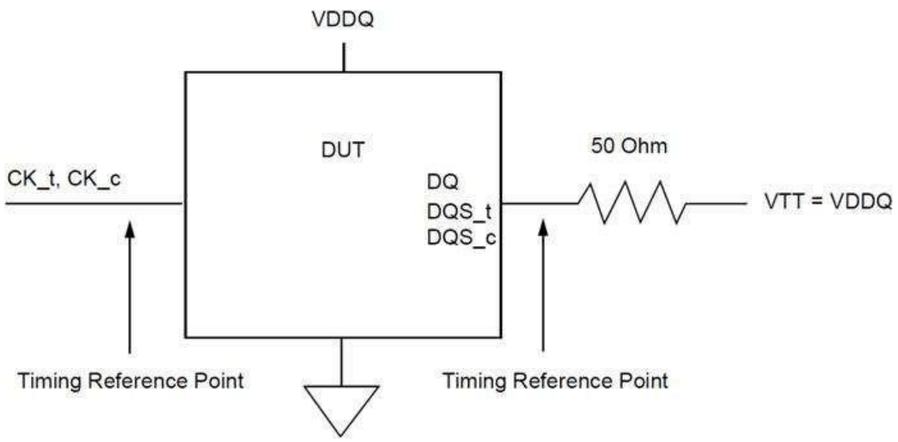
1. Package implementations shall meet spec if the Zpkg and Pkg Delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum value shown.
2. It is assumed that Lpkg can be approximated as Lpkg = Zo*Td.
3. It is assumed that Cpkg can be approximated as Cpkg = Td/Zo.

Electrical Characteristics & AC Timing

Reference Load for AC Timing and Output Slew Rate

Figure below represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined.

tREFI by device density

Parameter	Symbol		2Gb	4Gb	8Gb	16Gb	Unit
All Bank Refresh to active/refresh cmd time	tRFC		160	260	350	550	ns
Average periodic refresh interval	tREFI	0°C≤TCASE ≤85°C	7.8	7.8	7.8	7.8	µs
		-40°C≤TCASE ≤85°C	7.8	7.8	7.8	7.8	µs
		85°C≤TCASE ≤95°C	3.9	3.9	3.9	3.9	µs

NOTE:

Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if the devices support these options or requirements.

Timing Parameters by Speed Grade

Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2400

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	1.25	1.9	1.071	1.9	0.937	1.9	0.833	1.9	ps	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK (AVG) MAX + tJITper_tot MAX								tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-63	63	-54	54	-47	47	-42	42	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-31	31	-27	27	-23	23	-21	21	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-50	50	-43	43	-38	38	-33	33	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	-	125	-	107	-	94	-	83	ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	-	63	-	54	-	47	-	42	ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	100	-	86	-	75	-	67	ps	
Cumulative error across 2 cycles	tERR(2per)	-92	92	-79	79	-69	69	-61	61	ps	
Cumulative error across 3 cycles	tERR(3per)	-109	109	-94	94	-82	82	73	73	ps	
Cumulative error across 4 cycles	tERR(4per)	-121	121	-104	104	-91	91	-81	81	ps	
Cumulative error across 5 cycles	tERR(5per)	-131	131	-112	112	-98	98	-87	87	ps	
Cumulative error across 6 cycles	tERR(6per)	-139	139	-119	119	-104	104	-92	92	ps	
Cumulative error across 7 cycles	tERR(7per)	-145	145	-124	124	-109	109	-97	97	ps	
Cumulative error across 8 cycles	tERR(8per)	-151	151	-129	129	-113	113	-101	101	ps	
Cumulative error across 9 cycles	tERR(9per)	-156	156	-134	134	-117	117	-104	104	ps	
Cumulative error across 10 cycles	tERR(10per)	-160	160	-137	137	-120	120	-107	107	ps	
Cumulative error across 11 cycles	tERR(11per)	-164	164	-141	141	-123	123	110	110	ps	
Cumulative error across 12 cycles	tERR(12per)	-168	168	-144	144	-126	126	-112	112	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR*n*per MIN = (1 + 0.68ln[*n*]) × tJITper_tot MIN; tERR*n*per MAX = (1 + 0.68ln[*n*]) × tJITper_tot MAX								UI	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base, AC100)	115	-	100	-	80	-	62	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	215	-	200	-	180	-	162	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base, DC75)	140	-	125	-	105	-	87	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	215	-	200	-	180	-	162	-	ps	
Control and Address Input pulse width for each input	tIPW	600	-	525	-	460	-	410	-	ps	
Command and Address Timing											
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5nCK ,6.250 ns)	-	max(5nCK ,5.355 ns)	-	max(5nCK ,5.355 ns)	-	max(5nCK , 5 ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK	34

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing											
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (2K)	Max(4nCK ,6ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK , 5.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (1K)	Max(4nCK ,5ns)	-	Max(4nCK ,4.2ns)	-	Max(4nCK ,3.7ns)	-	Max(4nCK , 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK ,5ns)	-	Max(4nCK ,4.2ns)	-	Max(4nCK ,3.7ns)	-	Max(4nCK , 3.3ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK ,7.5ns)	-	Max(4nCK ,6.4ns)	-	Max(4nCK ,6.4ns)	-	Max(4nCK , 6.4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK ,6ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK , 4.9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK ,6ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK ,5.3ns)	-	Max(4nCK , 4.9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nC K,35ns)	-	Max(28nC K,30ns)	-	Max(28nC K,30ns)	-	Max(28nC K,30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nC K,25ns)	-	Max(20nC K,23ns)	-	Max(20nC K,21ns)	-	Max(20nC K ,21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nC K,20ns)	-	Max(16nC K,17ns)	-	Max(16nC K,15ns)	-	Max(16nC K,13ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK ,2.5ns)	-	max(2nCK ,2.5ns)	-	max(2nCK ,2.5ns)	-	max(2nCK , 2.5ns)	-	ns	1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK ,7.5ns)	-	max(4nCK ,7.5ns)	-	max(4nCK ,7.5ns)	-	max (4nCK,7.5 ns)	-	ns	1,3,4
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK ,7.5ns)	-	max(4nCK ,7.5ns)	-	max(4nCK ,7.5ns)	-	max(4nCK ,7.5ns)	-	ns	34
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nCK,3.7 5ns)	-	tWR+max (5nCK,3.7 5ns)	-	tWR+max (5nCK,3.7 5ns)	-	tWR+max (5nCK,3.7 5ns)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ max(4nCK , 3.75ns)	-	tWTR_S+ max(5nCK , 3.75ns)	-	tWTR_S+ max(5nCK , 3.75ns)	-	tWTR_S+ max(5nCK , 3.75ns)	-	ns	2, 29, 34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ max(4nCK , 3.75ns)	-	tWTR_L+ max(5nCK , 3.75ns)	-	tWTR_L+ max(5nCK , 3.75ns)	-	tWTR_L+ max(5nCK , 3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	597	-	597	-	768	-	768	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nC K,15ns)	-	max(24nC K,15ns)	-	max(24nC K,15ns)	-	max(24nC K, 15ns)	-	nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI	46,47

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CS_n to Command Address Latency											
CS_n to Command Address Latency	tCAL	max(3nCK ,3.748 ns)	-	max(3nCK ,3.748 ns)	-	max(3nCK ,3.748 ns)	-	max(3nCK ,3.748 ns)	-	nCK	
Mode Register Set cycle time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing											
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	-	0.16	-	0.16	-	0.17	tCK(avg)/ 2	13,18,39,49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.76	-	0.76	-	0.76	-	0.74	-	tCK(avg)/ 2	13,17,18,39,49
Data Valid Window per device: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	0.63	-	0.63	-	0.64	-	0.64	-	UI	17,18,39,49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.66	-	0.66	-	0.69	-	0.72	-	UI	17,18,39,49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-450	225	-390	195	-360	180	-330	175	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	225	-	195	-	180	-	175	ps	39
Data Strobe Timing											
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	39,40
		NA	NA	NA	NA	NA	NA	1.8	NOTE 44	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK	42
		NA	-	NA	-	NA	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-390	195	-360	180	330	175	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	225	-	195	-	180	-	175	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing lo-catino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	-225	225	-195	195	-180	180	175	175	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	370	-	330	-	310	-	290	ps	37,38,39

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
MPSM Timing											
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (min)	-	tCKSRX (min)	-	tCKSRX (min)	-	tCKSRX (min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL (min)	-	tXMP(min) + tXSDLL (min)	-	tXMP(min) + tXSDLL (min)	-	tXMP(min) + tXSDLL (min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-		
Calibration Timing											
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing											
Exit Reset from CKE HIGH to a valid command	tXPR	Max(5nCK ,tRFC(min) +10ns)	-	Max(5nCK ,tRFC(min) +10ns)	-	Max(5nCK ,tRFC(min) +10ns)	-	Max(5nCK ,tRFC(min) +10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	tRFC(min) +10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	tCKE(min) + 1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK ,10ns)+PL	-	max(5nCK ,10ns)+PL	-	max(5nCK ,10ns)+PL	-	max(5nCK ,10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	max(5nCK ,10ns)	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing											
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK ,6ns)	-	max(4nCK ,6ns)	-	max(4nCK ,6ns)	-	max(4nCK ,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK , 5ns)	-	max(3nCK , 5ns)	-	max(3nCK , 5ns)	-	max(3nCK , 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, C4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	nCK	
PDA Timing											
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		nCK	
ODT Timing											
Asynchronous RTT turn-on delay (Power- Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power- Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing											
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/ DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
CA Parity Timing											
Commands not guaranteed to be executed during this time	tPAR_ UNKNOWN	-	PL	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_ PW	48	96	56	112	64	128	72	144	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_ RSP	-	43	-	50	-	57	-	64	nCK	
Parity Latency	PL	4		4		4		5		nCK	
CRC Error Reporting											
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_ PW	6	10	6	10	6	10	6	10	nCK	
Geardown timing (Not Supported Below DDR4-2666)											
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	NA		NA		NA		NA			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	NA		NA		NA		NA			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	NA		NA		NA		NA			27
Sync pulse to First valid command(T4)	tCMD_GEAR	NA		NA		NA		NA			27
Geardown setup time	tGEAR_setup	NA	-	NA	-	NA	-	NA	-	nCK	
Geardown hold time	tGEAR_hold	NA	-	NA	-	NA	-	NA	-	nCK	
tREFI											
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	260	-	ns	34

Timing Parameters by Speed Bin for DDR4-2666 to DDR4-3200

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	ns	
Average Clock Period	tCK(avg)	0.750	<0.833	0.682	<0.750	0.625	<0.682	ps	35,36
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	MIN = tCK (AVG) MIN + tJITper_tot MIN; MAX = tCK (AVG) MAX + tJITper_tot MAX						tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	-38	38	-34	34	-32	32	ps	23
Clock Period Jitter- deterministic	JIT(per)_dj	-19	19	-17	17	-16	16	ps	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-30	30	-27	27	-25	25	ps	
Cycle to Cycle Period Jitter	tJIT(cc)_total	-	75	-	68	-	62	ps	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	-	38	-	-	-	-	ps	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	-	60	-	55	-	50	ps	
Cumulative error across 2 cycles	tERR(2per)	-55	55	-50	50	-46	46	ps	
Cumulative error across 3 cycles	tERR(3per)	-66	66	-60	60	-55	55	ps	
Cumulative error across 4 cycles	tERR(4per)	-73	73	-66	66	-61	61	ps	
Cumulative error across 5 cycles	tERR(5per)	-78	78	-71	71	-65	65	ps	
Cumulative error across 6 cycles	tERR(6per)	-83	83	-75	75	-69	69	ps	
Cumulative error across 7 cycles	tERR(7per)	-87	87	-79	79	-73	73	ps	
Cumulative error across 8 cycles	tERR(8per)	-91	91	-83	83	-76	76	ps	
Cumulative error across 9 cycles	tERR(9per)	-94	94	-85	85	-78	78	ps	
Cumulative error across 10 cycles	tERR(10per)	-96	96	-88	88	-80	80	ps	
Cumulative error across 11 cycles	tERR(11per)	-99	99	-90	90	-83	83	ps	
Cumulative error across 12 cycles	tERR(12per)	-101	101	-92	92	-84	84	ps	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR*nper* MIN = (1 + 0.68ln[*n*]) × tJITper_tot MIN tERR*nper* MAX = (1 + 0.68ln[*n*]) × tJITper_tot MAX						UI	
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base, AC90)	55	-	48	-	40	-	ps	
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	145	-	138	-	130	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base, DC65)	80	-	73	-	65	-	ps	
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	145	-	138	-	130	-	ps	
Control and Address Input pulse width for each input	tIPW	385	-	365	-	350	-	ps	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5nCK , 5ns)	-	max(5nCK , 5ns)	-	max(5nCK , 5ns)	-	nCK	34
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (2K)	Max(4nCK,5 .3ns)	-	Max(4nCK,5 .3ns)	-	Max(4nCK,5 .3ns)	-	nCK	34

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S (1K)	Max(4nCK,3 ns)	-	Max(4nCK,2 .7ns)	-	Max(4nCK,2 .5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,3 ns)	-	Max(4nCK,2 .7ns)	-	Max(4nCK,2 .5ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6 .4ns)	-	Max(4nCK,6 .4ns)	-	Max(4nCK,6 .4ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4 .9ns)	-	Max(4nCK,4 .9ns)	-	Max(4nCK,4 .9ns)	-	nCK	34
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,4 .9ns)	-	Max(4nCK,4 .9ns)	-	Max(4nCK,4 .9ns)	-	nCK	34
Four activate window for 2KB page size	tFAW_2K	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	ns	34
Four activate window for 1KB page size	tFAW_1K	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	ns	34
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK, 12ns)	-	Max(16nCK, 10.875ns)	-	Max(16nCK, 10ns)	-	ns	34
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2 .5ns)	-	max(2nCK,2 .5ns)	-	max(2nCK,2 .5ns)	-	ns	1,2,34
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	ns	1,34
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	max(4nCK,7 .5ns)	-	ns	34
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nCK,3.75n s)	-	tWR+max (5nCK,3.75n s)	-	tWR+max (5nCK,3.75n s)	-	ns	1,28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+ max(4nCK, 3.75ns)	-	tWTR_S+ max(5nCK, 3.75ns)	-	tWTR_S+ max(5nCK, 3.75ns)	-	ns	2,29,34
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+ max(5nCK, 3.75ns)	-	tWTR_L+ max(5nCK, 3.75ns)	-	tWTR_L+ max(5nCK, 3.75ns)	-	ns	3,30,34
DLL locking time	tDLLK	1024	-	1024	-	1024	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	nCK	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	nCK	
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))						nCK	
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	UI	45,47
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	UI	46,47

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
CS_n to Command Address Latency	tCAL	max(3nCK,3 .748 ns)	-	max(3nCK,3 .748 ns)	-	max(3nCK,3 .748 ns)	-	nCK	
Mode Register Set cyce time in CAL mode	tMRD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
Mode Register Set update delay in CAL mode	tMOD_tCAL	tMOD+ tCAL	-	tMOD+ tCAL	-	tMOD+ tCAL	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.18	-	0.19	-	0.22	tCK(avg)/ 2	13,18,39, 49
DQ output hold per group, per access from DQS_t,DQS_c	tQH	0.74	-	0.74	-	0.74	-	tCK(avg)/ 2	13,17,18, 39,49
Data Valid Window per device: (tQH - tDQSQ) of each UI on a given DRAM	tDVWd	TBD	-	TBD	-	TBD	-	UI	17,18,39, 49
Data Valid Window , per pin per UI : (tQH - tDQSQ) each UI on a pin of a given DRAM	tDVWp	0.72	-	0.72	-	0.72	-	UI	17,18,39, 49
DQ low impedance time from CK_t, CK_c	tLZ(DQ)	-310	170	-280	165	-250	160	ps	39
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	-	170	-	165	-	160	ps	39
Data Strobe Timing									
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	NOTE 44	0.9	NOTE 44	0.9	NOTE 44	tCK	39,40
		1.8	NOTE 44	1.8	NOTE 44	NA	NA	tCK	39,41
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	NOTE 45	0.33	NOTE 45	0.33	NOTE 45	tCK	39
DQS_t,DQS_c differential output high time	tQSH	0.4	-	0.4	-	0.4	-	tCK	21,39
DQS_t,DQS_c differential output low time	tQSL	0.4	-	0.4	-	0.4	-	tCK	20,39
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK	42
		1.8	-	1.8	-	1.8	-	tCK	43
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	tCK	
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-310	170	-280	165	-250	160	ps	39
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	170	-	165	-	160	ps	39
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	tCK	
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK	
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	0.18	-	0.18	-	tCK	
DQS_t, DQS_c rising edge output timing lo-catino from rising CK_t, CK_c with DLL On mode	tDQSCK (DLL On)	170	170	-165	165	-160	160	ps	37,38,39
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	270	-	265	-	260	ps	37,38,39

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (min)	-	tCKSRX (min)	-	tCKSRX (min)	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL (min)	-	tXMP(min) + tXSDLL (min)	-	tXMP(min) + tXSDLL (min)	-		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	tISmin + tIHmin	-	tISmin + tIHmin	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	Max(5nCK,tRFC(min)+10ns)	-	Max(5nCK,tRFC(min)+10ns)	-	Max(5nCK,tRFC(min)+10ns)	-	nCK	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-	nCK	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	nCK	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing with CA Parity enabled	tCKESR_PAR	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	tCKE(min)+1nCK+PL	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	max(5nCK,10ns)+PL	-	nCK	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	nCK	
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(4nCK,6ns)	-	max(4nCK,6ns)	-	max(4nCK,6ns)	-	nCK	
CKE minimum pulse width	tCKE	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	max(3nCK, 5ns)	-	nCK	31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	nCK	6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	2	-	nCK	7

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, C4OTF)	tWRPDEN	WL+4+(tWR /tCK(avg))	-	WL+4+(tWR /tCK(avg))	-	WL+4+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR /tCK(avg))	-	WL+2+(tWR /tCK(avg))	-	WL+2+(tWR /tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	nCK	
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	nCK	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		nCK	
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.28	0.72	0.26	0.74	0.26	0.74	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling hold time from rising DQS_t/ DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_ UNKNOWN	-	PL	-	PL	-	PL	nCK	
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	nCK	
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_P W	80	160	88	176	96	192	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RS P	-	71	-	78	-	85	nCK	
Parity Latency	PL	5		6		6		nCK	

Speed		DDR4-2666		DDR4-2933		DDR4-3200		Unit	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	3	13	3	13	3	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
Geardown timing (Not Supported Below DDR4-2666)									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	tXPR		tXPR		tXPR			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	tXS		tXS		tXS			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	tMOD + 4CK		tMOD + 4CK		tMOD + 4CK			27
Sync pulse to First valid command(T4)	tCMD_GEAR	tMOD		tMOD		tMOD			27
Geardown setup time	tGEAR_setup	2CK	-	2CK	-	2CK	-	nCK	
Geardown hold time	tGEAR_hold	2CK	-	2CK	-	2CK	-	nCK	
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	34
	4Gb	260	-	260	-	260	-	ns	34
	8Gb	350	-	350	-	350	-	ns	34
	16Gb	550	-	550	-	550	-	ns	34
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	34
	4Gb	160	-	160	-	160	-	ns	34
	8Gb	260	-	260	-	260	-	ns	34
	16Gb	350	-	350	-	350	-	ns	34
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	34
	4Gb	110	-	110	-	110	-	ns	34
	8Gb	160	-	160	-	160	-	ns	34
	16Gb	260	-	260	-	260	-	ns	34

NOTE :

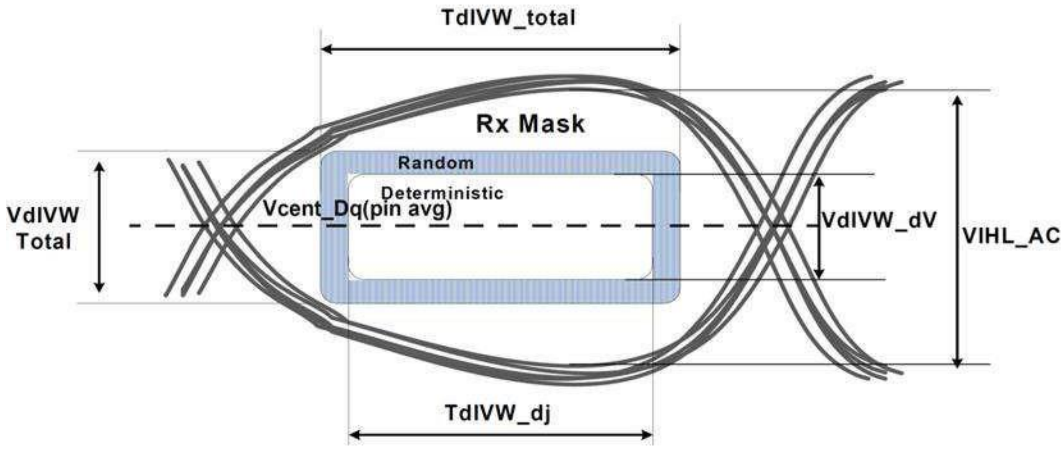
1. Start of internal write transaction is defined as follows : For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL. For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled.
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied.
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
14. The deterministic component of the total timing.
15. DQ to DQ static offset relative to strobe per group.
16. This parameter will be characterized and guaranteed by design.
17. When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock).
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are TBD.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks.
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
34. Parameters apply from tCK(avg)min to tCK(avg)max at all standard JEDEC clock period values as stated in the Speed Bin Tables.
35. This parameter must keep consistency with Speed-Bin Tables.
36. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate. UI=tCK(avg).min/2
37. applied when DRAM is in DLL ON mode.
38. Assume no jitter on input clock signals to the DRAM.
39. Value is only valid for RZQ/7 RONNOM = 34 ohms.

40. 1tCK toggle mode with setting MR4:A11 to 0.
41. 2tCK toggle mode with setting MR4:A11 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
42. 1tCK mode with setting MR4:A12 to 0.
43. 2tCK mode with setting MR4:A12 to 1, which is valid for DDR4-2400/2666/3200 speed grade.
44. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side.
45. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point.
46. last falling edge of DQS diff-signal cross-point to DQ rising signal middle-point of transferring from Low to High.
47. VrefDQ value must be set to either its midpoint or Vcent_DQ(midpoint) in order to capture DQ0 or DQL0 low level for entering PDA mode.
48. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side.
49. Reference level of DQ output signal is specified with a midpoint as a widest part of Output signal eye which should be approximately 0.7 * VDDQ as a center level of the static single-ended output peak-to-peak swing with a driver impedance of 34 ohms and an effective test load of 50 ohms to VTT = VDDQ.

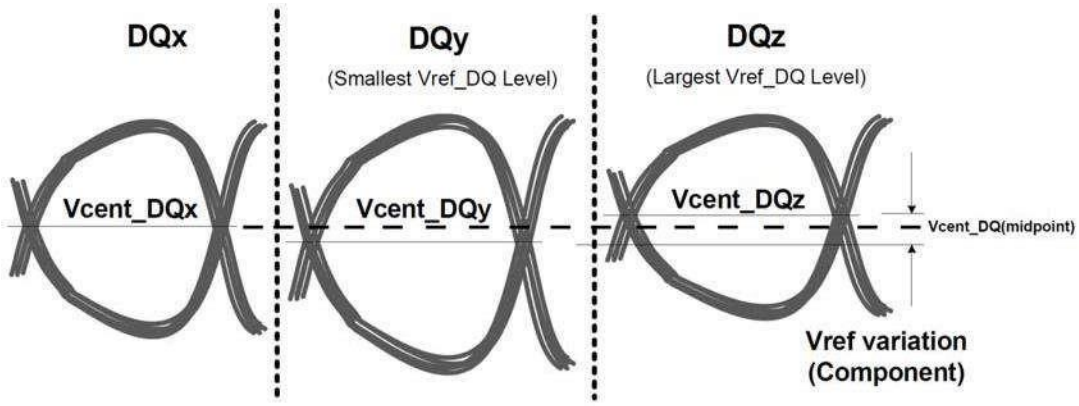
The DQ input receiver compliance mask for voltage and timing

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

DQ Receiver(Rx) compliance mask

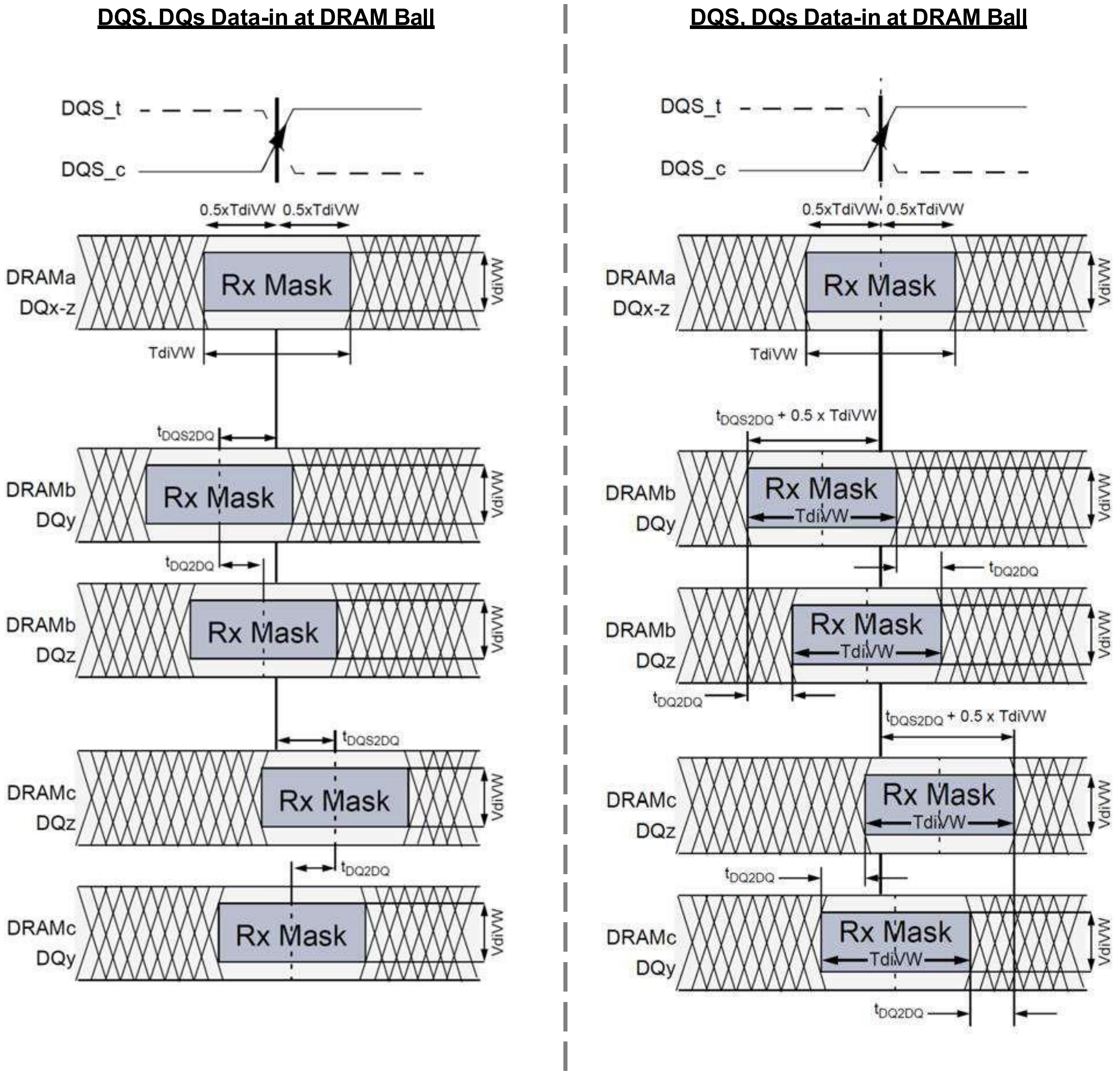


Across pin Vref DQ voltage variation



The Vref_DQ voltage is an internal reference voltage level that shall be set to the properly trained setting, which is generally Vcent_DQ(midpoint), in order to have valid Rx Mask values. Vcent_DQ is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DDR4 DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure “DQ Receiver(Rx) compliance mask”. This clarifies that any DDR4 DRAM component level variation must be accounted for within the DDR4 DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.

DQS to DQ and DQ to DQ Timings at DRAM Balls



Rx Mask

Rx Mask - Alternative View

NOTE :
DQx represents an optimally centered mask.
DQy represents earliest valid mask.

NOTE :
DRAMa represents a DRAM without any DQS/DQ skews.
DRAMb represents a DRAM with early skews (negative tDQS2DQ).

NOTE : Figures show skew allowed between DRAM to DRAM and DQ to DQ for a DRAM. Signals assume data centered aligned at DRAM Latch. TdiPW is not shown; composite data-eyes shown would violate TdiPW. VCENT DQ(midpoint) is not shown but is assummed to be midpoint of VdiVW.

All of the timing terms in the previous figure are measured at the VdIVW_total voltage levels centered around Vcent_DQ(midpoint) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.

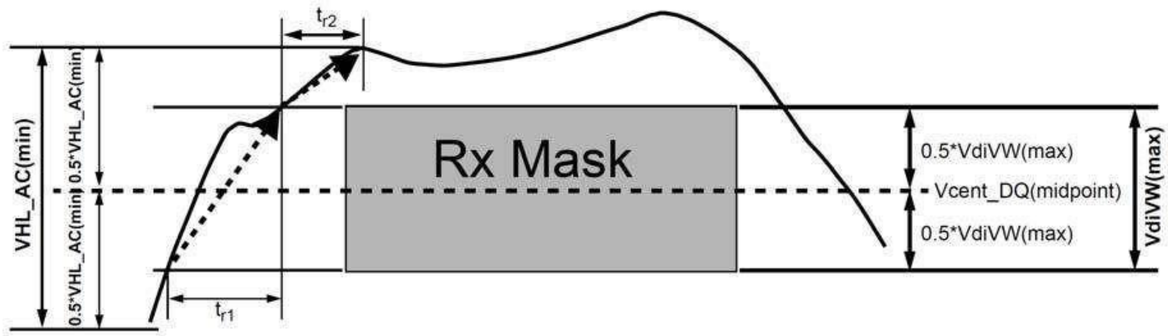
The rising edge slew rates are defined by srr1 and srr2. The slew rate measurement points for a rising edge are shown in Figure 5A below: A low to high transition tr1 is measured from 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) while tr2 is measured from the last transition through 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) above Vcent_DQ(midpoint).

Rising edge slew rate equations:

srr1 = VdIVW(max) / tr1

srr2 = (VIHL_AC(min) – VdIVW(max)) / (2*tr2)

Slew Rate Conditions For Rising Transition



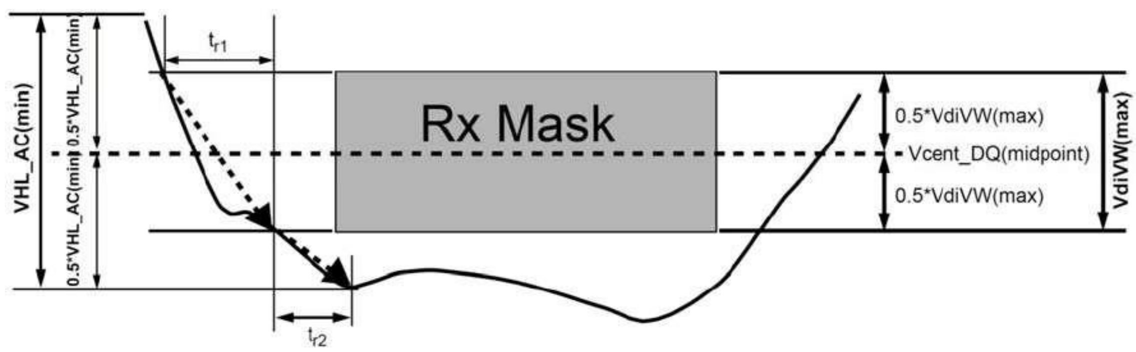
The falling edge slew rates are defined by srf1 and srf2. The slew rate measurement points for a falling edge are shown in Figure below: A high to low transition tf1 is measured from 0.5*VdiVW(max) above Vcent_DQ(midpoint) to the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) while tf2 is measured from the last transition through 0.5*VdiVW(max) below Vcent_DQ(midpoint) to the first transition through the 0.5*VIHL_AC(min) below Vcent_DQ(pin mid).

Falling edge slew rate equations:

srf1 = VdIVW(max) / tf1

srf2 = (VIHL_AC(min) – VdIVW(max)) / (2*tf2)

Slew Rate Conditions For Falling Transition



DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	DDR4-1600/ 1866/2133		DDR4-2400		DDR4-2666		DDR4-2933		DDR4-3200		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
VdiVW	Rx Mask voltage - pk-pk	-	136	-	130	-	120	-	115	-	110	mV	2,3
TdiVW	Rx timing window	-	0.2	-	0.2	-	0.22	-	0.23	-	0.23	UI	2,3
VIHL_AC	DQ AC input swing pk-pk	186	-	160	-	150	-	145	-	140	-	mV	4,5
TdiPW	DQ input pulse width	0.58	-	0.58	-	0.58	-	0.58	-	0.58	-	UI	6
tDQS2DQ	Rx Mask DQS to DQ offset	-0.17	0.17	-0.17	0.17	-0.19	0.19	-0.22	0.22	-0.22	0.22	UI	7
tDQ2DQ	Rx Mask DQ to DQ offset	-	TBD	-	TBD	-	0.115	-	0.115	-	0.125	UI	8
srr1, srf1	Input Slew Rate over Vdlvw if tCK >=0.935ns	1	9	1	9	1	9	1	9	1	9	V/ns	9
	Input Slew Rate over Vdivw if tCK>=0.625ns	-	-	1.25	9	1.25	9	1.25	9	1.25	9	V/ns	9
srr2	Rising Input Slew Rate over 1/2 VIHL_AC	0.2 x srr1	9	0.2 x srr1	9	0.2 x srr1	9	0.2 x srr1	9	0.2 x srr1	9	V/ns	10
srf2	Falling Input Slew Rate over 1/2 VIHL_AC	0.2 x srf1	9	0.2 x srf1	9	0.2 x srf1	9	0.2 x srf1	9	0.2 x srf1	9	V/ns	10

NOTE
1. All Rx mask specifications must be satisfied for each UI. For example, if the minimum input pulse width is violated when satisfying TdiVW (MIN), VdiVW,max, and minimum slew rate limits, then either TdiVW (MIN) or minimum slew rates would have to be increased to the point where the minimum input pulse width would no longer be violated.
2. Data Rx mask voltage and timing total input valid window where VdiVW is centered around VCENTDQ,midpoint after VREFDQ training is completed. The data Rx mask is applied per bit and should include voltage and temperature drift terms. The input buffer design specification is to achieve at least a BER =1e- 16 when the Rx mask is not violated.
3. Defined over the DQ internal VREF range 1.
4. Overshoot and undershoot specifications apply.
5. DQ input pulse signal swing into the receiver must meet or exceed VIHL(AC)min. VIHL(AC)min is to be achieved on an UI basis when a rising and falling edge occur in the same UI (a valid TdiPW).
6. DQ minimum input pulse width defined at the VCENTDQ,midpoint.
7. DQS-to-DQ Rx mask offset is skew between DQS and DQ within a nibble (x4) or word (x8, x16 [for x16, the upper and lower bytes are treated as separate x8s]) at the SDRAM balls over process, voltage, and temperature.
8. DQ-to-DQ Rx mask offset is skew between DQs within a nibble (x4) or word (x8, x16) at the SDRAM balls for a given component over process, voltage, and temperature.
9. Input slew rate over VdiVW mask centered at VCENTDQ,midpoint. Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within 1.7V/ns of each other.
10. Input slew rate between VdiVW mask edge and VIHL(AC)min points.

DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	X4	X8	X16
Write Leveling	V	V	V
Temperature controlled Refresh	V	V	V
Low Power Auto Self Refresh	V	V	V
Fine Granularity Refresh	V	V	V
Multi Purpose Register	V	V	V
Data Mask		V	V
Data Bus Inversion		V	V
TDQS		V	
ZQ calibration	V	V	V
DQ Vref Training	V	V	V
Per DRAM Addressability	V	V	V
Mode Register Readout	V	V	V
CAL	V	V	V
WRITE CRC	V	V	V
CA Parity	V	V	V
Control Gear Down Mode	V	V	V
Programmable Preamble	V	V	V
Maximum Power Down Mode	V	V	
Boundary Scan Mode			V
Additive Latency	V	V	

Revision History

Revision	Date	Notes
1.0	Apr. 22,2026	New issue