



High Speed Super Low Power SRAM

32K-Word By 8 Bit

CS18LV02560

Revision History

Rev. No.	History	Issue Date
1.0	Initial issue with new naming rule	Aug. 18, 2011
1.1	Remove 28-PDIP Package	May. 25, 2012
1.2	Change 28L TSOP18x13.4mm package outline	Dec. 10, 2019



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GENERAL DESCRIPTION

The CS18LV02560 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 32,768 words by 8bits and operates for a single 2.7 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide both high speeds, super low power features. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE).

The CS18LV02560 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV02560 is available in JEDEC standard 28-pin TSOP I (8x13.4 mm), SOP (330 mil) packages.

FEATURES

- Wide operation voltage : 2.7V ~ 5.5V
- Ultra low power consumption :
 - 2mA@1MHz (Max.), Vcc=5.0V.
 - 10 uA (Max.) CMOS standby current
- High speed access time: 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 2.0V.
- Easy expansion with /CE and /OE options.



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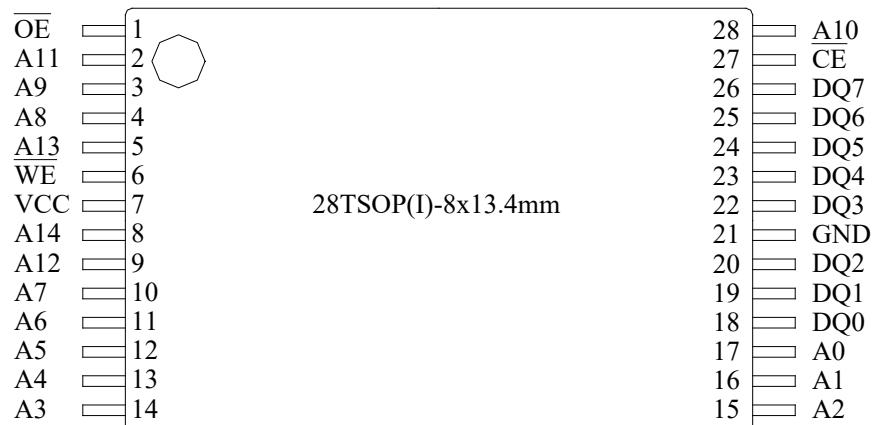
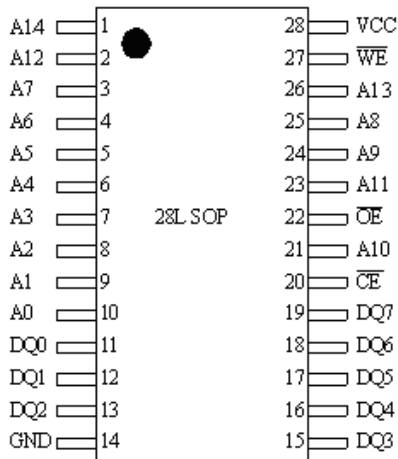
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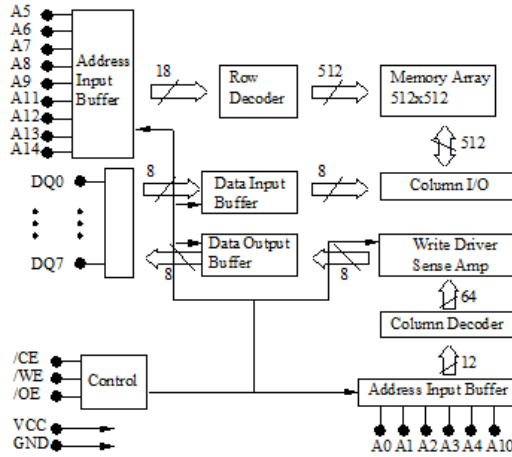
PRODUCT FAMILY

Product Family	Operating Temp	V _{CC} Range	Speed (ns)	Standby (Typ.)	Package Type
CS18LV02560	0~70°C	2.7~5.5	55/70	1.5 uA (V _{CC} = 5.0V)	28 SOP
					28 TSOP I
					Dice
	-40~85°C	2.7~5.5	55/70	2.0 uA (V _{CC} = 5.0V)	28 SOP
					28 TSOP I
					Dice

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A14	Input	Address inputs for selecting one of the 32,768 x 8 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground



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TRUTH TABLE

Mode	/CE	/WE	/OE	DQ0~7	V _{CC} Current
Standby	H	X	X	High Z	I _{CCSB} , I _{CCSB1}
Output Disabled	L	H	H	High Z	I _{CC}
Read	L	H	L	D _{OUT}	I _{CC}
Write	L	L	X	D _{IN}	I _{CC}

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Symbol	Parameter	Rating	Unit
V _{CC}	Supply voltage, V _{CC}	-0.5 to +7	V
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7	V
T _{BIAS}	Temperature under Bias	-40 to +125	°C
T _{STG}	Storage Temperature	-60 to +150	°C
P _T	Power Dissipation	1.0	W
I _{OUT}	DC Output Current	20	MA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	V _{CC}
Commercial	0~70°C	2.7~5.5V
Industrial	-40~85°C	2.7~5.5V



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CAPACITANCE ⁽¹⁾ ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter	Conduction	MAX.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	6	pF
C_{DQ}	Input/output Capacitance	$V_{I/O} = 0V$	8	pF

1. This parameter is guaranteed, and not 100% tested.

DC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$, $V_{CC} = 5.0/3.0V$)

Name	Parameter	Test Condition	MIN	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage	$V_{CC} = 3.0V$	-0.5 ⁽¹⁾	0.8	V
V_{IH}	Guaranteed Input High Voltage	$V_{CC} = 5.0V$	2.2	$V_{CC} + 0.2$ ⁽²⁾	V
I_{IL}	Input Leakage Current	$V_{CC} = \text{MAX}$, $V_{IN} = 0$ to V_{CC}	-1	1	μA
I_{OL}	Output Leakage Current	$V_{CC} = \text{MAX}$, $/CE = V_{IN}$, or $/OE = V_{IN}$ $V_{IO} = 0V$ to V_{CC}	-1	1	μA
V_{OL}	Output Low Voltage	$V_{CC} = \text{MAX}$, $I_{OL} = 2.1\text{mA}$		0.4	V
V_{OH}	Output High Voltage	$V_{CC} = \text{MIN}$, $I_{OH} = -1\text{mA}$	2.4		V
I_{CC}	Operating Power Supply Current	$/CE = V_{IL}$, $I_{DQ} = 0\text{mA}$, $F = F_{\text{MAX}} = 1/t_{RC}$		30	mA
I_{CCSB}	TTL Standby Supply	$/CE = V_{IH}$, $I_{DQ} = 0\text{mA}$,		2.0	mA
I_{CCSB1}	CMOS Standby Current	$/CE \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$,		10	μA

1. Undershoot : -2.0V in case of pulse width 20ns

2. Overshoot : $V_{CC} + 2.0V$ in case of pulse width 20ns



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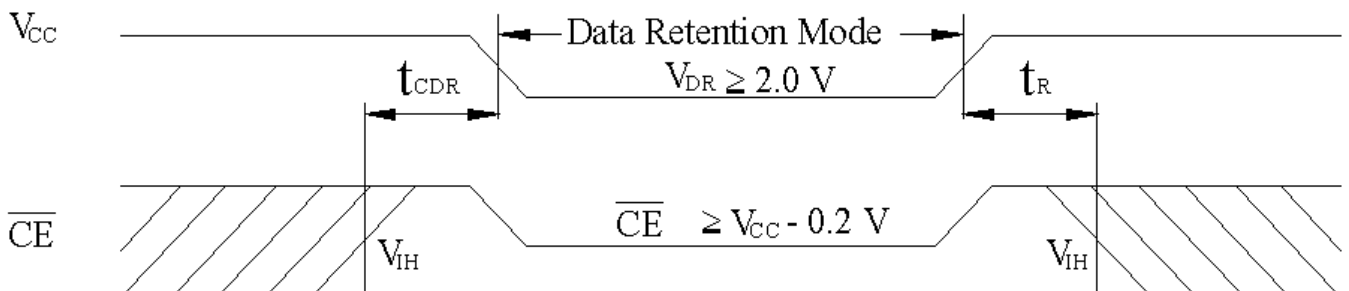
DATA RETENTION CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$)

Name	Parameter	Test Condition	MIN	Typ (2)	MAX	Unit
VDR	VCC for Data Retention	$/\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	2.0			V
ICCDR	Data Retention Current	$/\overline{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$, $V_{\text{CC}} = 2\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$		0.5	2.0	μA
TCDR	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (1)			ns

1. t_{RC} = Read Cycle Time.

2. $T_A = 25^\circ\text{C}$

LOW V_{CC} DATA RETENTION WAVEFORM (/CE Controlled)



AC TEST CONDITIONS

Input Pulse Levels	$V_{CC}/0V$
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	$0.5V_{CC}$

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS

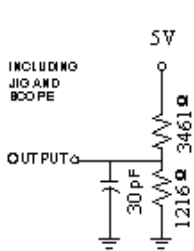


FIGURE 1A

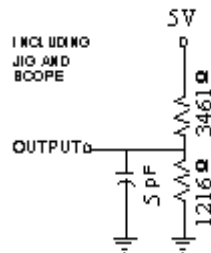


FIGURE 1B

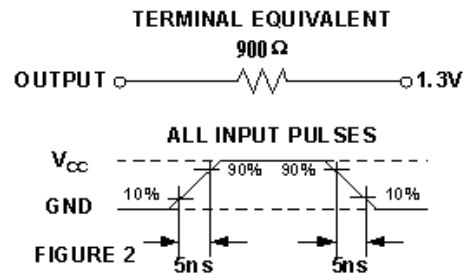


FIGURE 2



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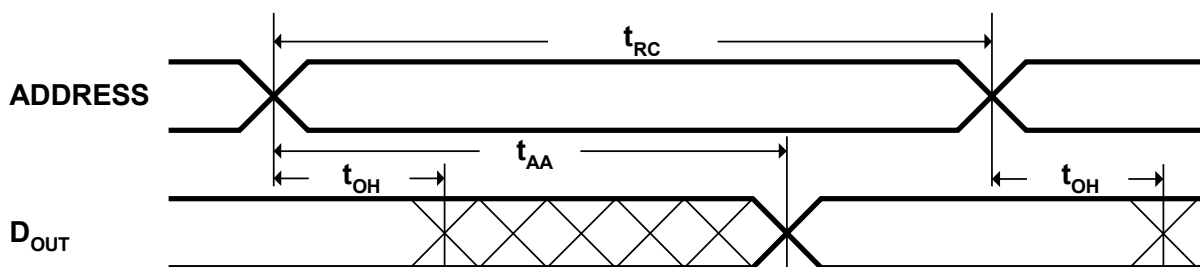
AC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

< READ CYCLE >

JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
tAVAX	t _{RC}	Read Cycle Time	55		70		ns
tAVQV	t _{AA}	Address Access Time		55		70	ns
tELQV	t _{ACE}	Chip Select Access Time		55		70	ns
tGLQV	t _{OE}	Output Enable to Output Valid		30		50	ns
tELQX	t _{CLZ}	Chip Select to Output Low Z	10		10		ns
tGLQX	t _{OLZ}	Output Enable to Output in Low Z	5		5		ns
tEHQZ	t _{CHZ}	Chip Deselect to Output in High Z	0	35	0	35	ns
tGHQZ	t _{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
tAXOX	t _{OH}	Address Change to Out Disable	10		10		ns

SWITCHING WAVEFORMS (READ CYCLE)

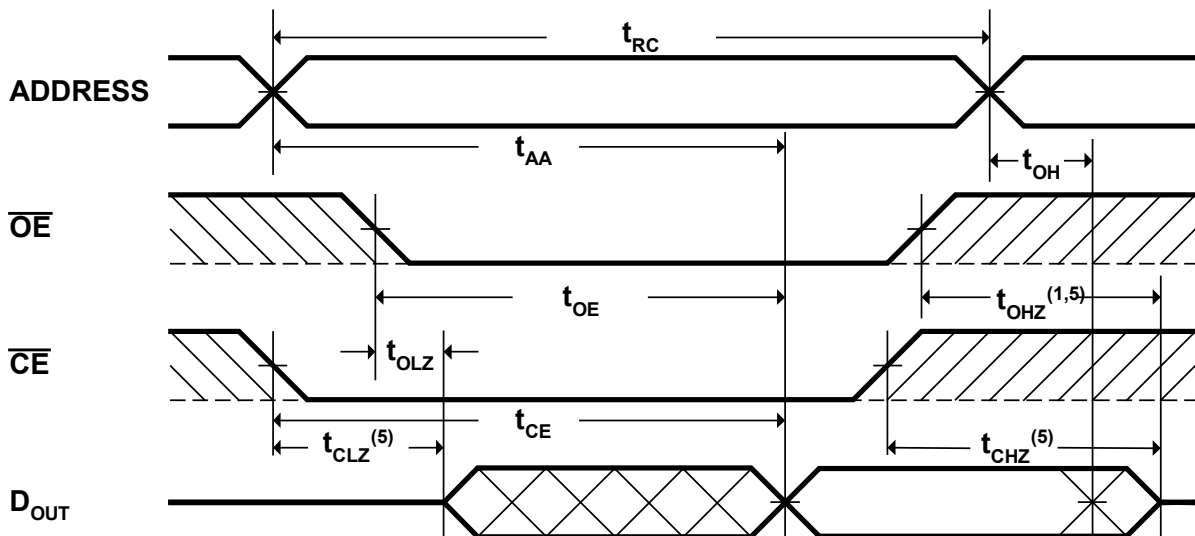
READ CYCLE1 (1, 2, 4)



READ CYCLE2 (1, 3, 4)



READ CYCLE3 (1, 4)



NOTES:

1. /WE is high in read Cycle.
2. Device is continuously selected when /CE = V_{IL}.
3. Address valid prior to or coincident with CE transition low.
4. /OE = V_{IL}.
5. Test conditions assume signal transition times of 5ns or less, timing reference levels of 0.5V_{CC}, input pulse levels of 0V to V_{CC} and output loading specified in Figure 1A.



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6. Transition is measured $\pm 500\text{mV}$ from steady state with $C_L = 5\text{pF}$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.

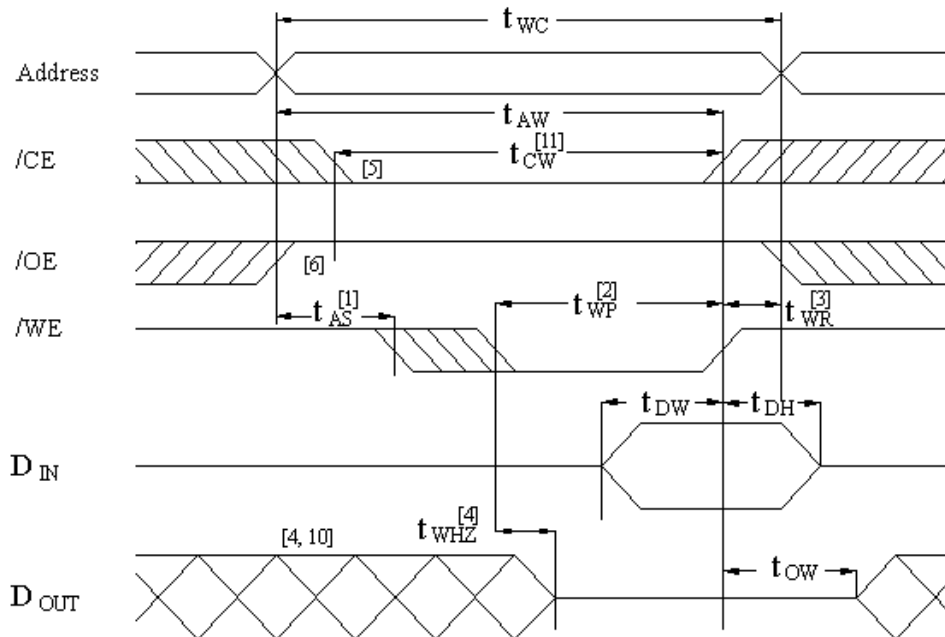
AC ELECTRICAL CHARACTERISTICS ($T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

< WRITE CYCLE >

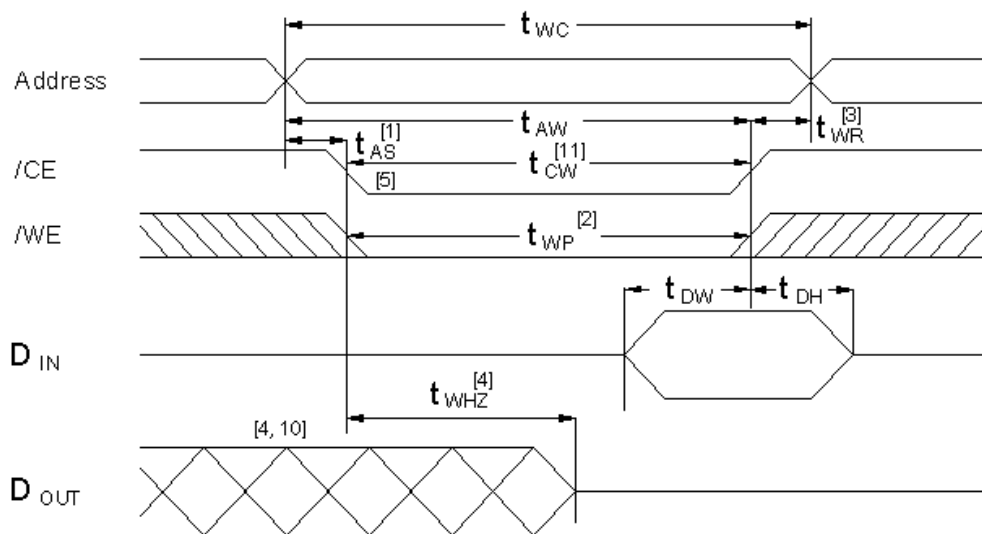
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
tAVAX	tWC	Write Cycle Time	55		70		ns
tE1LWH	tCW	Chip Select to End of Write	55		70		ns
tAVWL	tAS	Address Setup Time	0		0		ns
tAVWH	tAW	Address Valid to End of Write	55		70		ns
tWLWH	tWP	Write Pulse Width	40		50		ns
tWHAX	tWR	Write Recovery Time	0		0		ns
tWLQZ	tWHZ	Write to Output in High Z		25		35	ns
tDVWH	tDW	Data to Write Time Overlap	20		30		ns
tWHDX	tDH	Data Hold for Write End	0		0		ns
tGHQZ	tOHZ	Output Disable to Output in High Z	0	30	0	30	ns
tWHOX	tOW	End of Write to Output Active	5		5		ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



WRITE CYCLE2 (Chip Enable Controlled)





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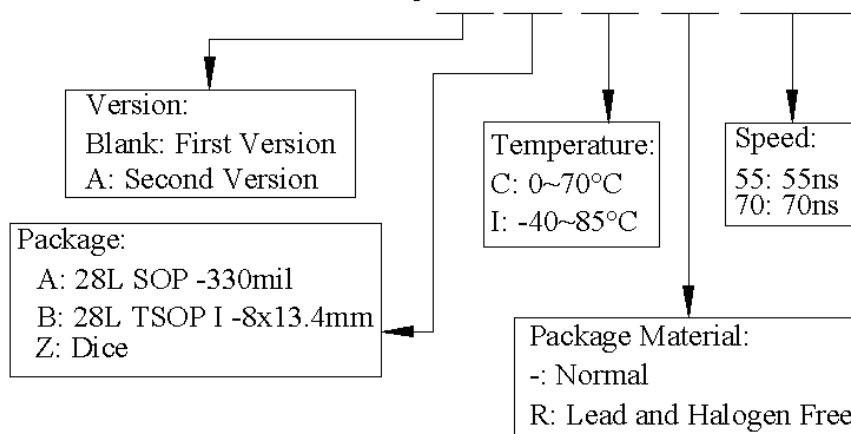
CS18LV02560

NOTES:

1. /WE must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. TWR is measured from the earlier of /CE or /WE going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.
6. It's recommended to keep /OE at high (V_{IH}) as /WE Controlled WRITE CYCLE.
7. DOUT is the read data of next address.
8. If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Test conditions assume signal transition times of 5ns or less, timing reference levels of $0.5V_{CC}$, input pulse levels of 0V to V_{CC} and output loading specified in Figure 1A.
10. Transition is measured $\pm 500mV$ from steady state with $CL = 5pF$ as shown in Figure 1B. The parameter is guaranteed but not 100% tested.
11. TCW is measured from the later of /CE going low to the end of write.

ORDER INFORMATION

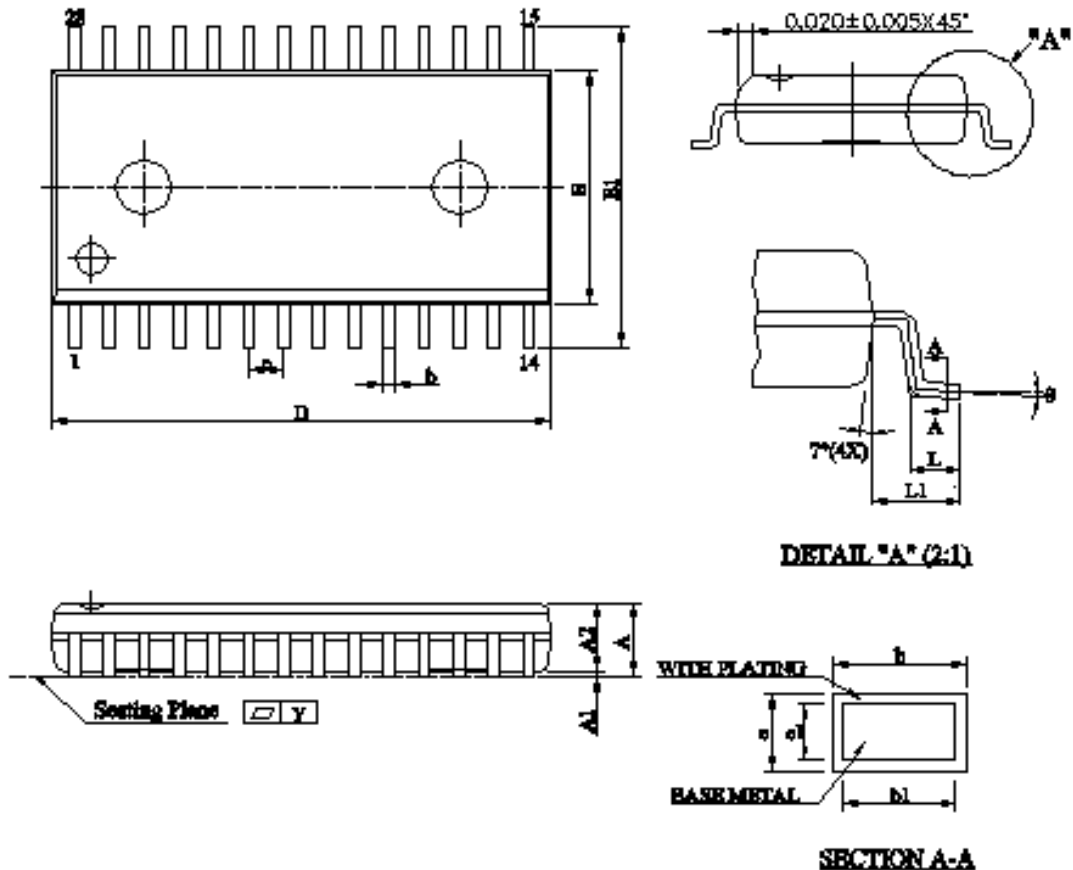
CS18LV02560X X X X XX



Note: Package material code "R" meets ROHS

PACKAGE OUTLINE

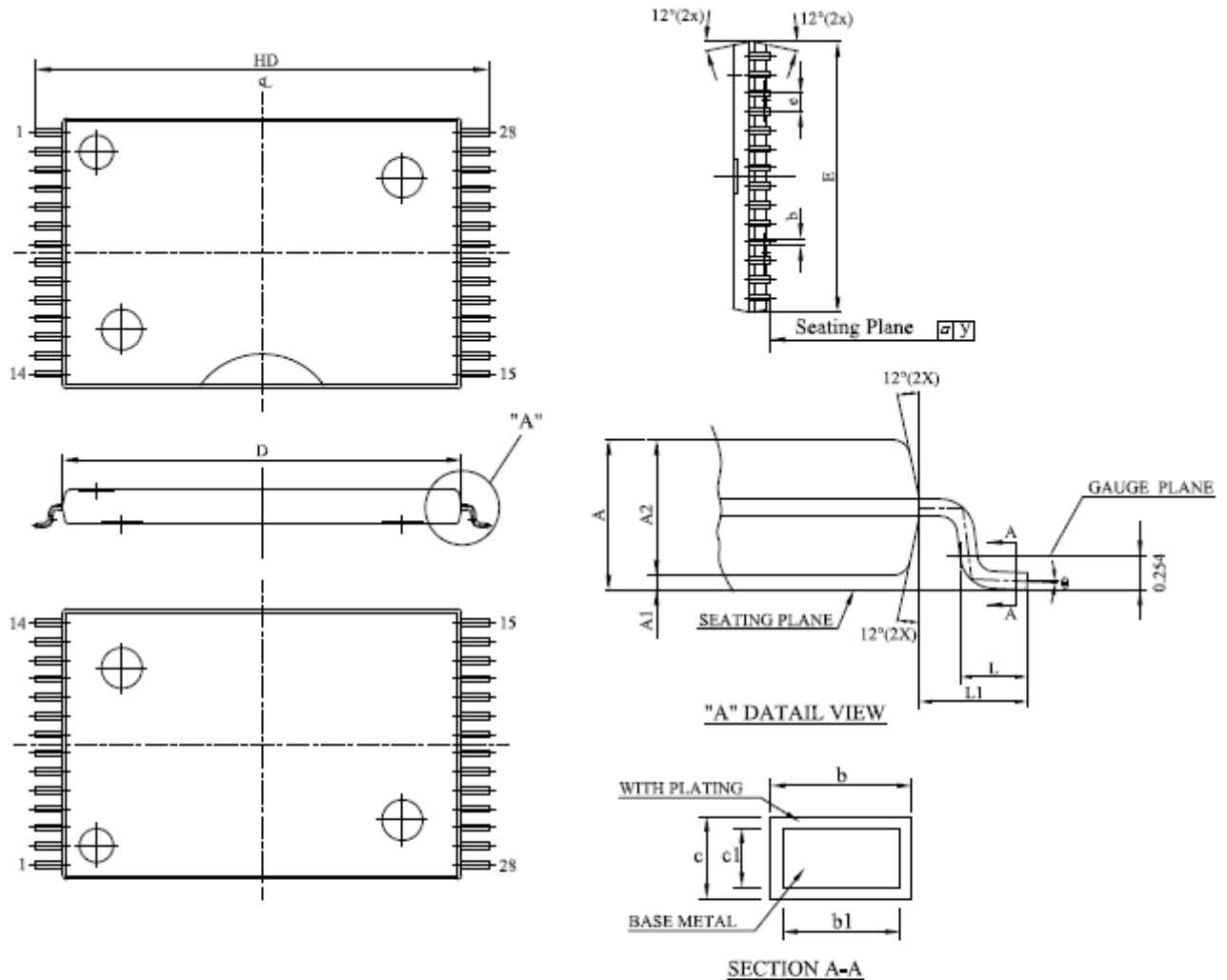
28L SOP-330mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	B
mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	-	0°
	Nom.	2.692	0.226	2.489	-	-	-	-	18.110	8.407	11.811	1.270	0.964	1.720	-	-
	Max.	2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	-	0°
	Nom.	0.106	0.009	0.098	-	-	-	-	0.713	0.331	0.465	0.050	0.0380	0.0677	-	-
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

28L TSOP(I)-8x13.4mm



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
UNIT																
mm	Min.	1.00	0.050	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.45	13.20	0.40	0.70	-	0°
	Nom.	1.10	0.115	1.00	0.22	0.20	-	-	11.80	8.00	0.55	13.40	0.50	0.80	-	-
	Max.	1.20	0.180	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.65	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.0019	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.018	0.520	0.0157	0.0275	-	0°
	Nom.	0.0433	0.0045	0.039	0.009	0.008	-	-	0.465	0.315	0.022	0.528	0.0197	0.0315	-	-
	Max.	0.0473	0.0071	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.026	0.536	0.0277	0.0355	0.004	8°