Revision History

Rev. No.	**History**	**Issue Date**
1.0	New Issue	Jun.29, 2005
1.1	Add a new 32L WSON-8x8mm package	Jun.29, 2005
1.2	Revise I_{CCSB1} Typ	Apr. 07, 2006
1.3	Remove WSON	June.12, 2006
1.4	Add I_{CCSB1} Typ 3uA	Jul. 28, 2015
1.5	New package outline added for 32L sTSOP(I)-8x13.4mm	Nov. 15, 2017

High Speed Super Low Power SRAM

128K Word By 8 Bit

CS18LV10245

GENERAL DESCRIPTION

The CS18LV10245 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 131,072 words by 8bits and operates from a wide range of 4.5 to 5.5V supply voltage. Advanced CMOS technology and circuit techniques provide high speed, super low power features and maximum access time of 55/ 70ns in 5.0V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1, CE2) and active LOW output enable (/OE).

The CS18LV10245 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS18LV10245 is available in JEDEC standard 32-pin sTSOP 1- 8x13.4 mm, TSOP 1- 8x20mm, TSOP 2- 400mil , SOP-450 mil, PDIP- 600 mil.

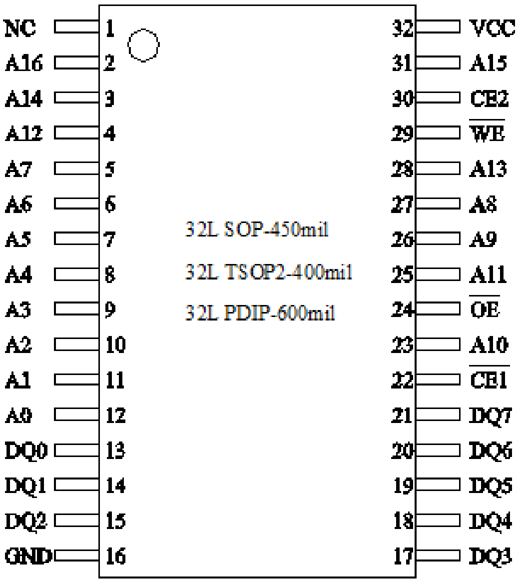
FEATURES

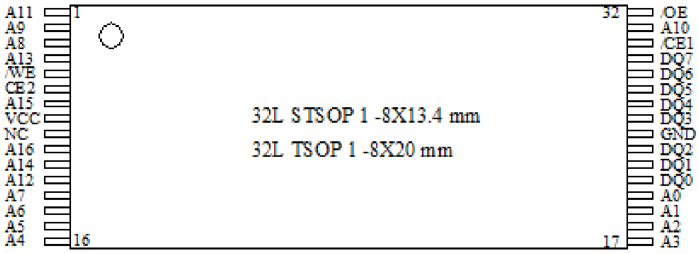
- Wide operation voltage: 4.5~5.5V
- Ultra-low power consumption : 2mA@1MHz (Max.), V_{CC}=5.0V.
- High speed access time: 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supplies voltage as low as 2.0V.
- Easy expansion with (/CE1, CE2) and /OE options.

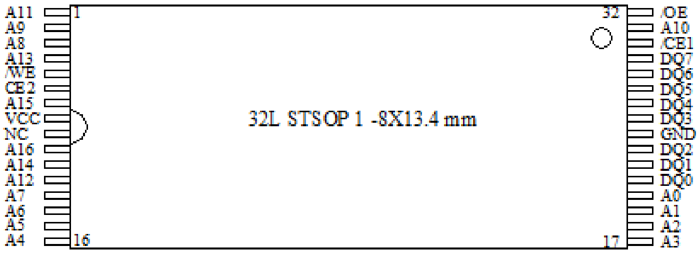
Product Family

Part No.	Operating Temp	Standby (Max) (V_{CC} = 5.0V)	V_{CC}. Range	Speed (ns)	Package Type
CS18LV10245	0~70°C	10uA	4.5~5.5	55/ 70	32L SOP
					32L STSOP 1
					32L TSOP 1
	-40~85°C	15uA			32L TSOP 2
					32L PDIP
					Dice

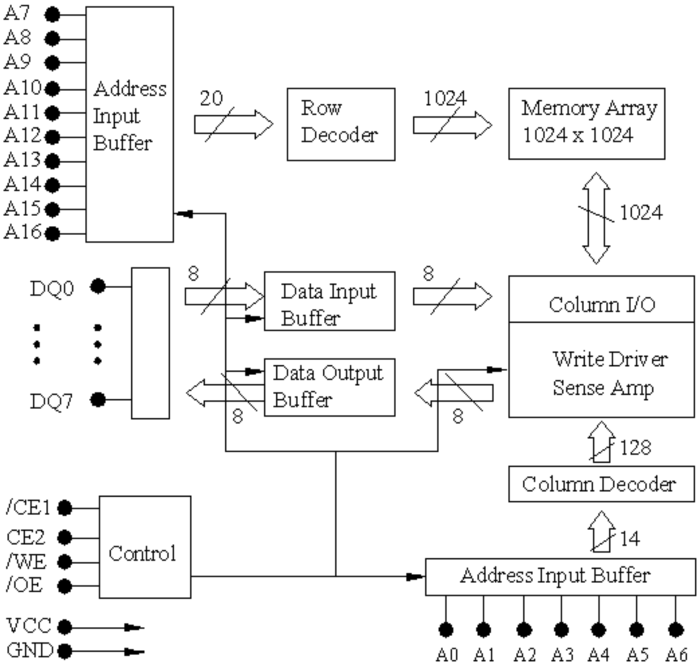
PIN CONFIGURATIONS







UNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A16	Input	Address inputs for selecting one of the 131,072 x 8 bit words in the RAM
/CE1, CE2	Input	/CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
DQ0~DQ7	I/O	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Gnd	Power	Ground
NC		No connection

TRUTH TABLE

MODE	/CE1	CE2	/WE	/OE	DQ0~7	Vcc Current
Standby	H	X	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	L	X	X		
Output Disable	L	H	H	H	High Z	I_{CC}
Read	L	H	H	L	D_{OUT}	I_{CC}
Write	L	H	L	X	D_{IN}	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70^{o}C	4.5~5.5V
Industrial	-40~85^{o}C	4.5~5.5V

1. Overshoot: V_{CC}+2.0V in case of pulse width ≦20ns.

2. Undershoot: - 2.0V in case of pulse width ≦20ns.

3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE (1) (T_A = 25℃, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not tested.

DC ELECTRICAL CHARACTERISTICS $(T_A = 0℃ \sim 70℃, V_{cc} = 5.0V)$

Name	Parameter	Test Condition	MIN	TYP[1]	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)	Vcc=5.0V	-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage (2)	Vcc=5.0V	2.2		Vcc+0.5	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE1=V_{Ih}, or CE2= $V_{IL,}$ or /OE=$V_{Ih,\ or}$ /WE= V_{IL} V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} =2.1mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1.0mA	2.4			V
I_{CC}	Operating Power Supply Current	/CE1=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}			30	mA
I_{CCSB}	TTL Standby Supply	/CE1=V_{IH}, I_{DQ}=0mA,			1.0	mA
I_{CCSB1}	CMOS Standby Current	/CE1≧V_{CC}-0.2V, CE2≦ 0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V,		3	10	uA

1. *Typical characteristics are at $T_A = 25℃$.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.*
3. *Fmax = $1/t_{RC.}$*

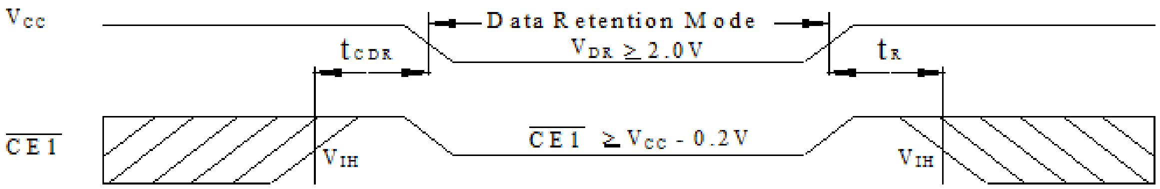
DATA RETENTION CHARACTERISTICS (T_A = 0℃ ~70℃, V_{CC} =5.0V)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE1≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	2.0			V
I_{CCDR}	Data Retention Current	VCC=2.0V, /CE1≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.5	5	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC}(2)			ns

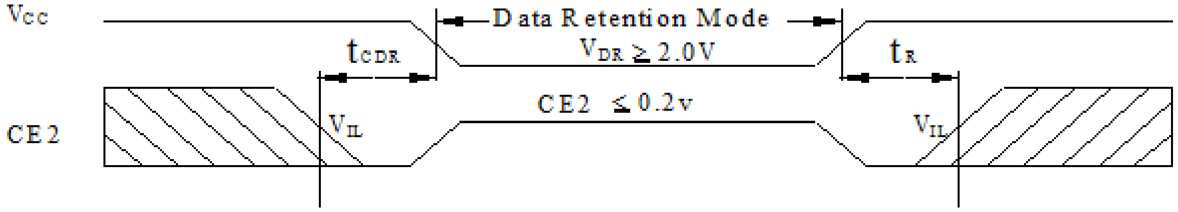
1. TA = 25℃

2. t_{RC}= .Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE1 Controlled)



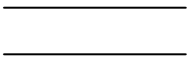
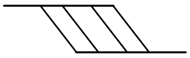
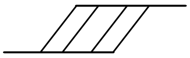
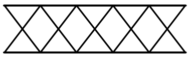
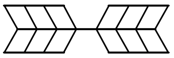
LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	See FIGURE 1A and 1B

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS

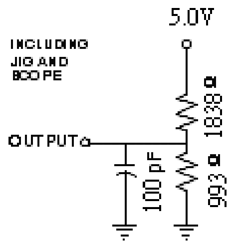


FIGURE 1A

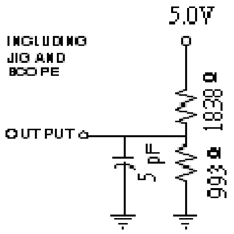


FIGURE 1B

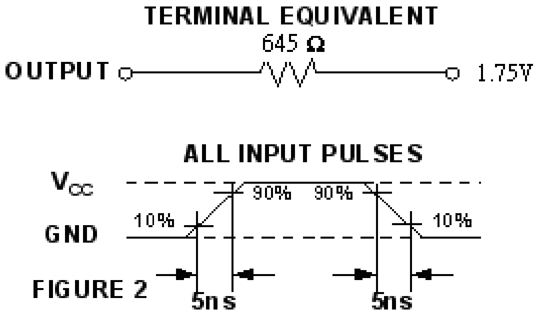


FIGURE 2

AC ELECTRICAL CHARACTERISTICS $(T_A = 0℃ \sim 70℃ ; V_{CC}=5.0V)$

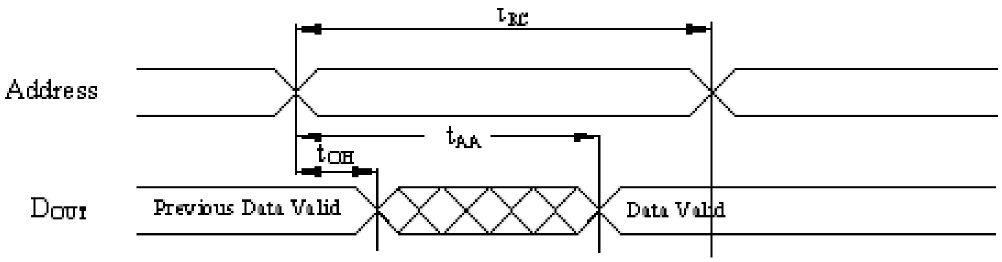
< READ CYCLE >

JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{ACE}	Chip Select Access Time		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		25		35	ns
t_{ELQX}	$t_{CLZ}^{(5)}$	Chip Select to Output Low Z	10		10		ns
t_{GLQX}	$t_{OLZ}^{(5)}$	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	$t_{CHZ}^{(5)}$	Chip Deselect to Output in High Z	0	20	0	25	ns
t_{GHQZ}	$t_{OHZ}^{(5)}$	Output Disable to Output in High Z	0	20	0	25	ns

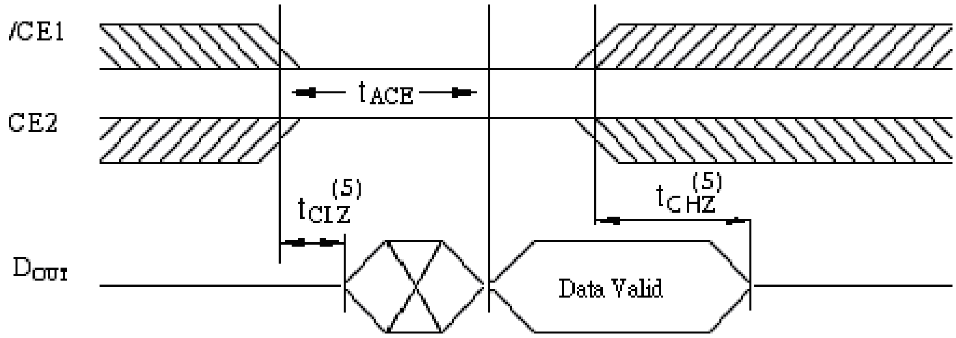
t_{AXOX}	t_{OH}	Address Change to Out Disable	10		10		ns

SWITCHING WAVEFORMS (READ CYCLE)

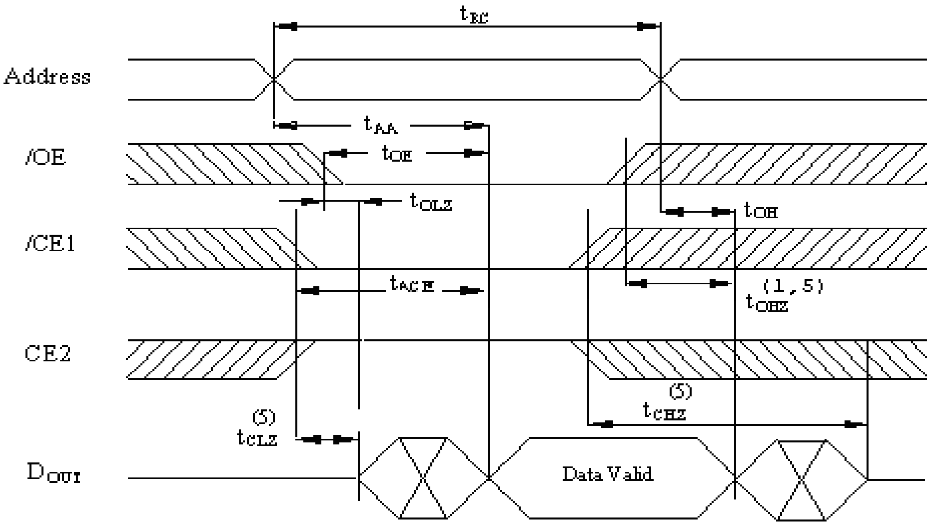
READ CYCLE 1 [1, 2, 4]



READ CYCLE 2 [1, 3, 4]



READ CYCLE 3 [1, 4]



NOTES:

1. */WE is high in read Cycle.*
2. *Device is continuously selected when /CE1 = VIL and CE2=VIH.*
3. *Address valid prior to or coincident with /CE1 transition low and /or CE2 transition high.*
4. */OE = VIL.*
5. *Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.*

AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃ ; V_{CC}=5.0V)

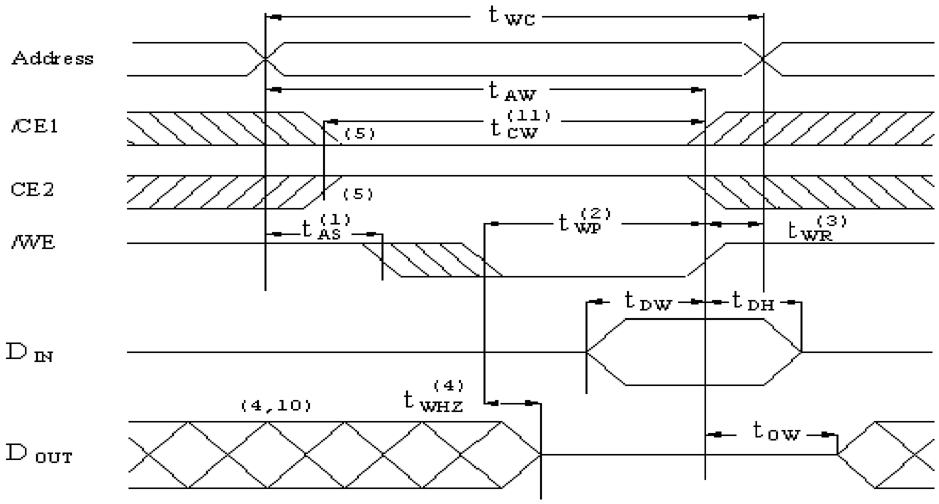
< WRITE CYCLE >

JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns

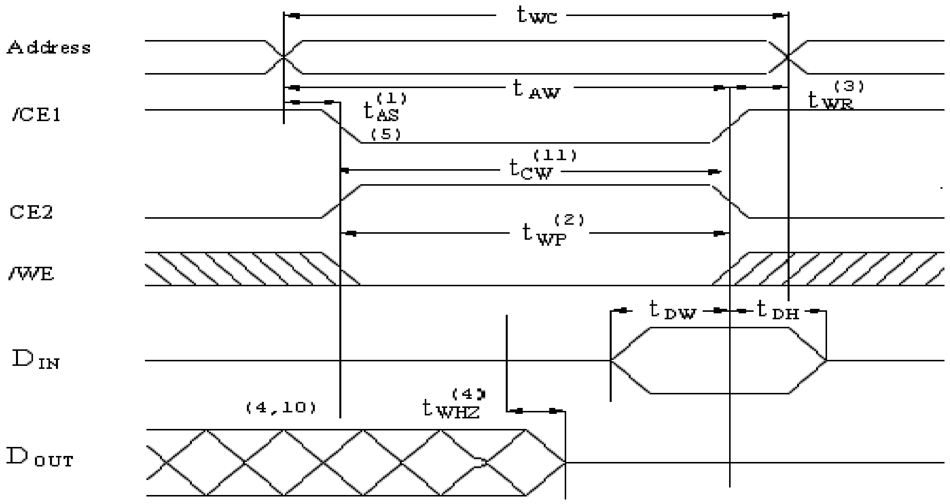
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}(10)	Write to Output in High Z		20		20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold for Write End	0		0		ns
t_{GHQZ}	t_{OHZ}(10)	Output Disable to Output in High Z	0	30	0	30	ns
t_{WHOX}	t_{OW}(10)	End of Write to Output Active	5		5		ns

SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (Write Enable Controlled)



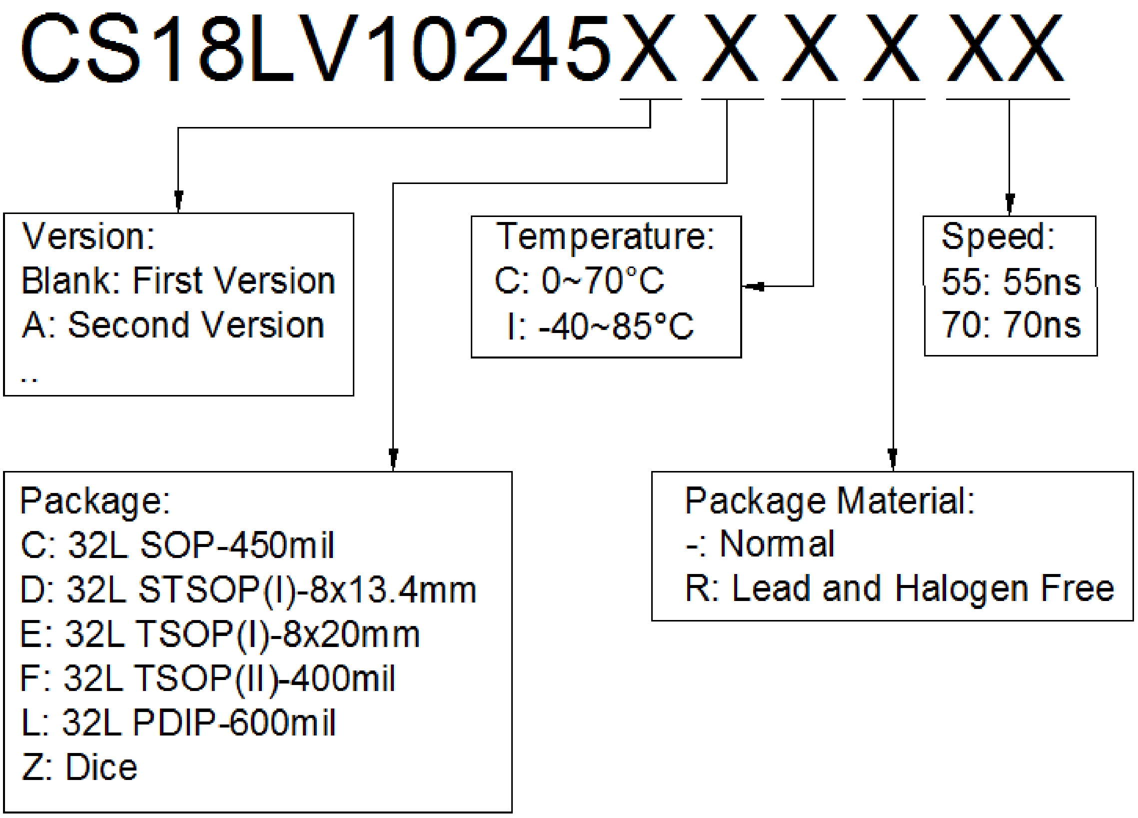
WRITE CYCLE2 (Chip Enable Controlled)



NOTES:

1. *TAS is measured from the address valid to the beginning of write.*
2. *The internal write time of the memory is defined by the overlap of /CE1 and CE2 active and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.*
3. *TWR is measured from the earlier of /CE1 or /WE going high or CE2 going low at the end of write cycle.*
4. *During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.*
5. *If the /CE1 low transition or CE2 high transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.*
6. */OE is continuously low (/OE = V_{IL}).*
7. *DOUT is the same phase of write data of this write cycle.*
8. *DOUT is the read data of next address.*
9. *If /CE1 is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.*
10. *Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.*
11. *TCW is measured from the later of /CE1 going low or CE2 going high to the end of write.*

ORDER INFORMATION



CS18LV10245X X X X XX

Version:
Blank: First Version
A: Second Version
..

Temperature:
C: 0~70°C
I: -40~85°C

Speed:
55: 55ns
70: 70ns

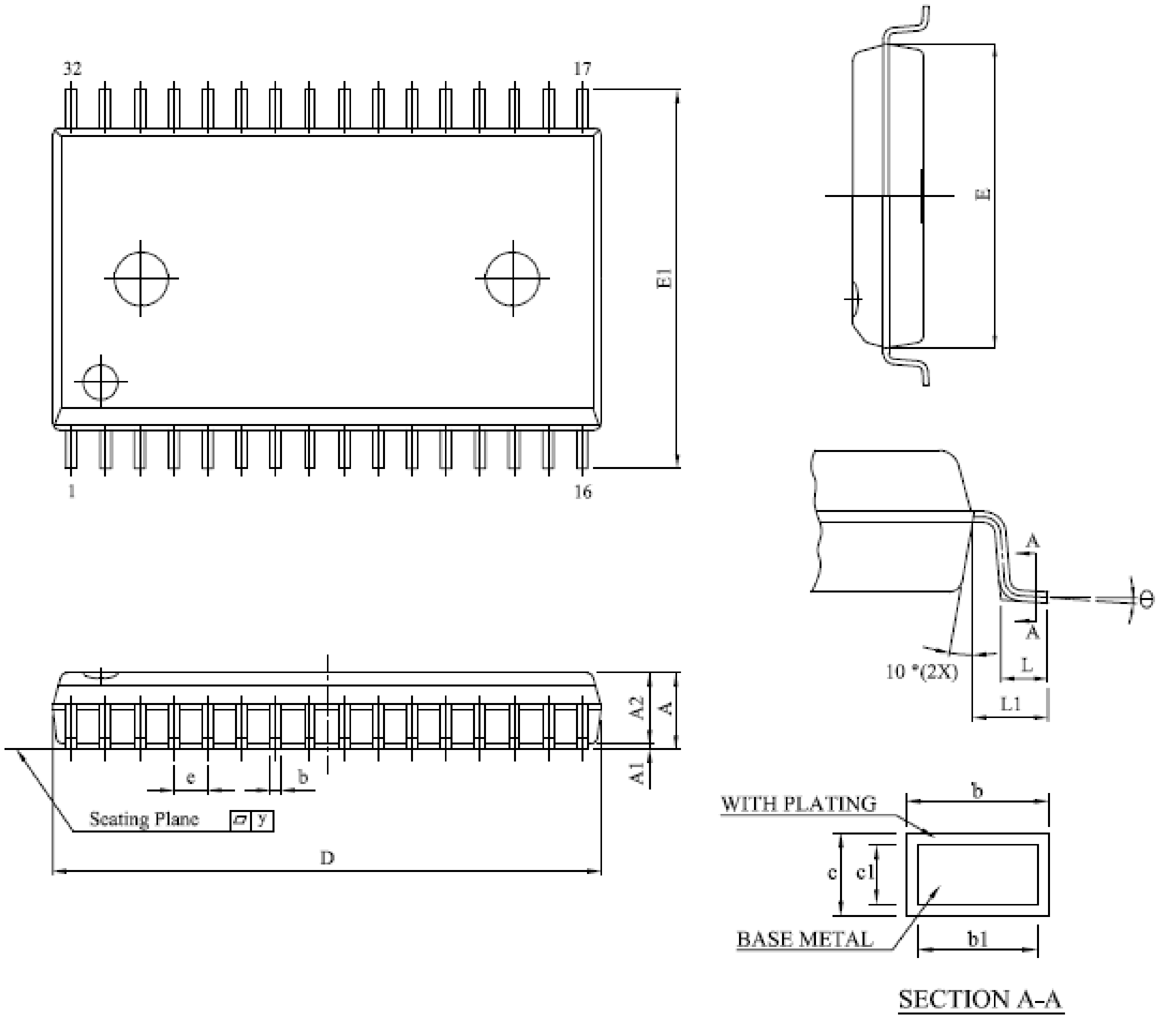
Package:
C: 32L SOP-450mil
D: 32L STSOP(I)-8x13.4mm
E: 32L TSOP(I)-8x20mm
F: 32L TSOP(II)-400mil
L: 32L PDIP-600mil
Z: Dice

Package Material:
-: Normal
R: Lead and Halogen Free

Note: Package material code “R” meets ROHS

PACKAGE OUTLINE

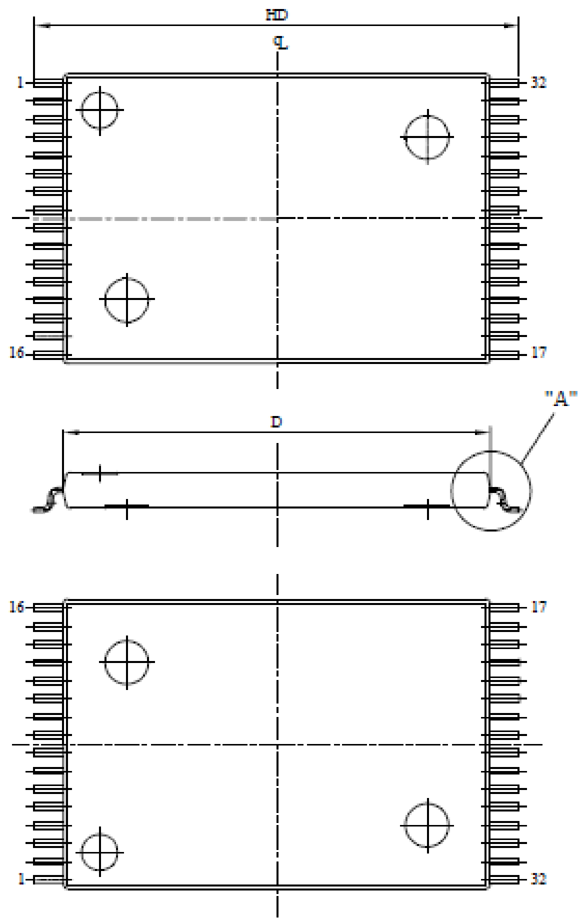
32L SOP-450mil

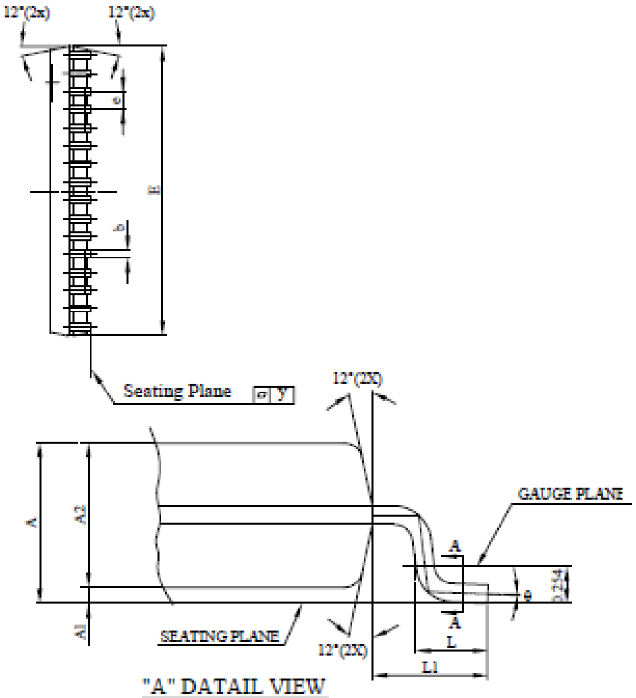


Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

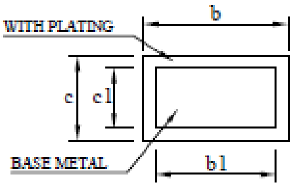
UNIT \ SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	–	0°
	Nom.	2.821	0.229	2.680	–	–	–	–	20.447	11.303	14.097	1.270	0.834	1.397	–	–
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	–	0°
	Nom.	0.111	0.009	0.1055	–	–	–	–	0.805	0.445	0.555	0.050	0.033	0.055	–	–
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

32L STSOP(I)-8x13.4mm (option 1)





"A" DATAIL VIEW

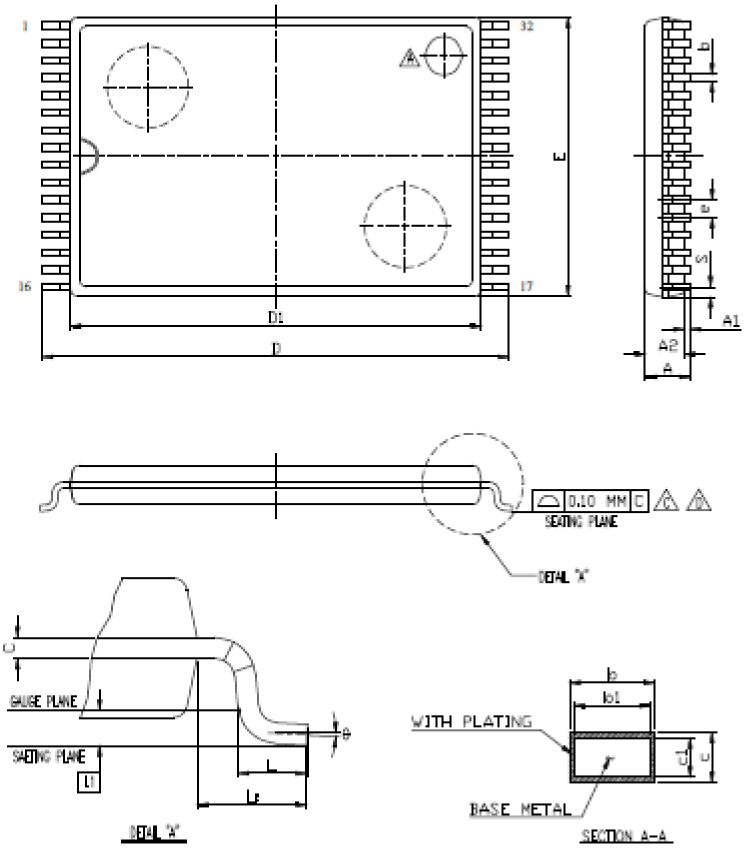


SECTION A-A

Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

UNIT \ SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.40	13.20	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	–	–	11.80	8.00	0.50	13.40	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.60	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.016	0.520	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	–	–	0.465	0.315	0.020	0.528	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.024	0.536	0.0277	0.0355	0.004	8°

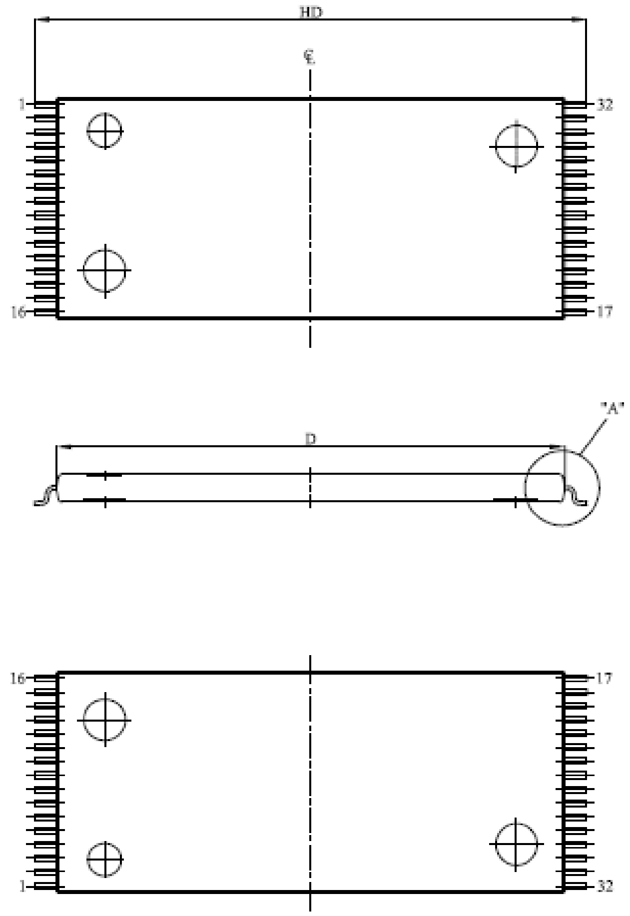
32L STSOP(I)-8x13.4mm (option 2)

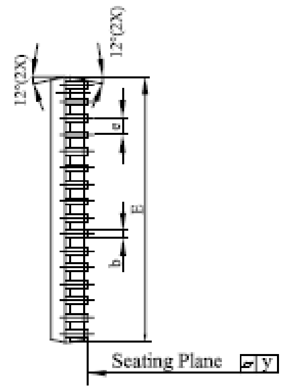


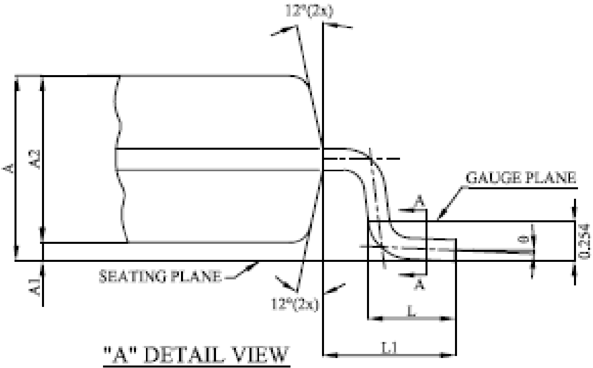
Note: Dimensions D1 and E do not include mold protrusions.
D1 and E are maximun plastic body size dimensions including mold mismatch.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	E	e	D	D1	L	L1	LE	S	Θ
mm	Min.		0.05	0.90	0.17	0.17	0.10	0.10	7.90	0.50 TYP.	13.20	11.70	0.30	0.25 BSC	0.675	0.278 TYP.	0
	Nom.			1.00	0.22	0.20	–	–	8.00		13.40	11.80	0.50				3
	Max.	1.20		1.05	0.27	0.23	0.21	0.16	8.10		13.60	11.90	0.70				5
inch	Min.		0.002	0.035	0.007	0.007	0.004	0.004	0.311	0.020 TYP.	0.520	0.461	0.012	0.010 BSC	0.027	0.0109 TYP.	0
	Nom.			0.039	0.009	0.008	–	–	0.315		0.528	0.465	0.020				3
	Max.	0.047		0.041	0.011	0.009	0.008	0.006	0.319		0.535	0.469	0.028				5

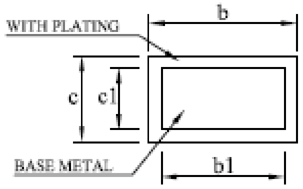
32L TSOP(I)-8x20mm







"A" DETAIL VIEW

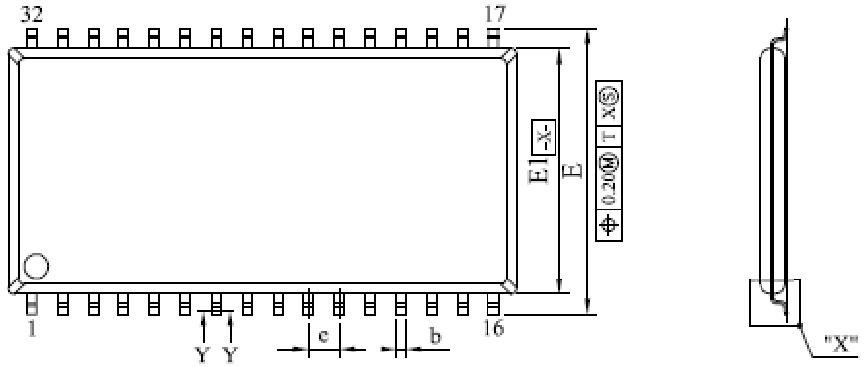


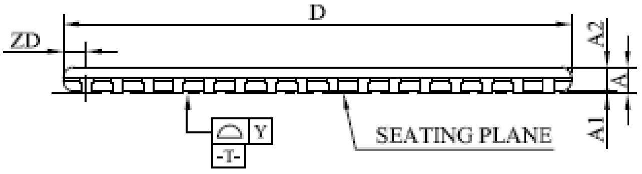
SECTION A-A

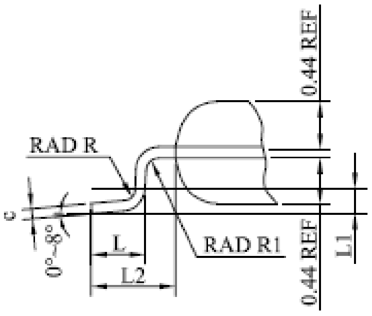
Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

UNIT \ SYMBOL		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	–	–	18.40	8.00	0.50	20.00	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	–	–	0.724	0.315	0.020	0.787	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

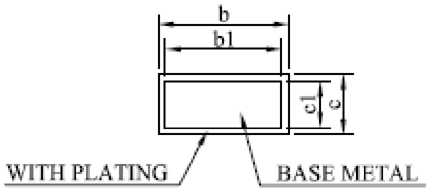
32L TSOP2-400mil







DETAIL "X"

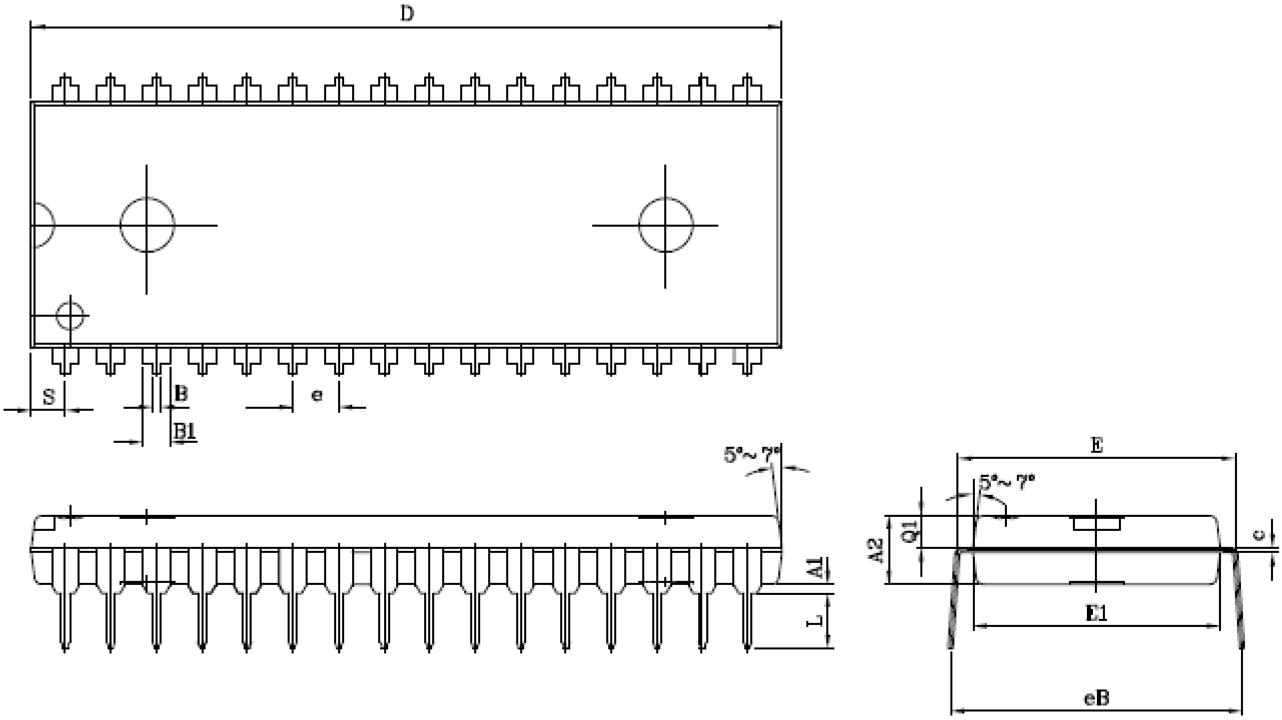


SECTION Y-Y

Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

UNIT \ SYMBOL		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	L2	R	R1	ZD	Y
mm	Min.	–	0.05	0.95	0.30	0.30	0.12	0.10	20.82	11.56	10.03	1.27 bsc	0.40	0.25 bsc	0.8 ref	0.12	0.12	0.95 ref	–
	Nom.	–	0.10	1.00	–	0.40	–	0.127	20.95	11.76	10.16		0.50			–	–		–
	Max.	1.20	0.15	1.05	0.52	0.45	0.21	0.16	21.08	11.96	10.29		0.60			0.25	–		0.10
inch	Min.	–	0.002	0.037	0.012	0.012	0.005	0.004	0.820	0.455	0.394	0.050 bsc	0.016	0.010 bsc	0.031 ref	0.005	0.005	0.037 ref	–
	Nom.	–	0.004	0.039	–	0.016	–	0.005	0.825	0.463	0.400		0.020			–	–		–
	Max.	0.047	0.006	0.042	0.020	0.018	0.008	0.006	0.830	0.471	0.405		0.024			0.010	–		0.004

32L PDIP-600mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

UNIT \ SYMBOL		A1	A2	B	B1	c	D	E	E1	e	eB	L	S	Q1
mm	Min.	0.254	3.785	0.330	1.143	0.152	41.783	14.986	13.716	2.540 (TYP)	16.002	3.048	1.651	1.651
	Nom.	–	3.912	0.457	1.270	0.254	41.910	15.240	13.818		16.510	3.302	1.905	1.778
	Max.	–	4.039	0.584	1.397	0.356	42.037	15.494	13.920		17.018	3.556	2.159	1.905
inch	Min.	0.010	0.149	0.013	0.045	0.006	1.645	0.590	0.540	0.100 (TYP)	0.630	0.120	0.065	0.065
	Nom.	–	0.154	0.018	0.050	0.010	1.650	0.600	0.544		0.650	0.130	0.075	0.070
	Max.	–	0.159	0.023	0.055	0.014	1.655	0.610	0.548		0.670	0.140	0.085	0.075