Cover Sheet and Revision Status				
版別 (Rev.)	DCC No	生效日 (Eff. Date)	變更說明 (Change Description)	發行人 (Originator)
1.0	20240011	Jul.-04 -2024	New issue	Hank Lin

General Description

The 64Mb OPI PSRAM (Pseudo Static RAM) is a low power, high-speed CMOS Double Data Rate, self- refresh DRAM with a low pin count Octal SPI Xccela interface.
The dynamic cell in the DRAM array needs to be refreshed periodically. Internal refresh control logic of PSRAM manages the refresh operation of array cell when the memory isn't actively engaged for reading or writing by the host. Since the host is not required to manage any refresh operations, the DRAM array seems to the host as if it employs static cells capable of retaining data without the need for refresh. Therefore, the memory is described as Pseudo Static RAM (PSRAM).
Octal SPI Xccela interface is a SPI-compatible low signal count, DDR interface supporting eight I/Os. The DDR protocol transmits two data bytes per clock cycle on the DQ[7:0] input/output signals. A read or write operation consists of a series of 16-bit wide, one clock cycle data transfers at the internal RAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible.

Features

- Interface and Power Supply
  - Octal SPI with DDR Xccela mode
  - VDD/VDDQ=1.62~1.98V / 2.7~3.6V
  - Output driver LVCMOS
  - Configurable output drive strength
- Performance
  - Clock rate up to 250MHz
  - Double data rate
  - Data throughput up to 500 MBps
- Organization
  - 64Mb, 8M x 8bits
  - 1024 bytes page size
  - Column address: AY0 to AY9
  - Row address: AX0 to AX12
- Self-managed refresh
- Hardware/Software Reset
- Power Saving Modes
  - Partial Array Self-Refresh
  - Auto temperature compensated self-refresh by built- in temperature sensor
  - Ultra low power Hybrid Sleep mode
  - User configurable refresh rate
  - Deep power down mode
- Write Burst Length
  - Minimum 2 Bytes
  - Maximum 1024 Bytes
- DQS/DM Pin
  - Output during read operation as Data Strobe (DQS)
  - Input during write operation as Data Mask (DM)
- Linear Burst Command
- Row boundary crossing supported for read operation via Mode Register

Programmable Functions

- Burst Type : Linear, Wrap, Hybrid wrap
- Burst Length : 16, 32, 64, 1K
- Driver Strength : 25, 50, 100, 200, 400 Ω
- Read/Write initial Latency : 3, 4, 5, 6, 7, 8, 9
- Refresh Rate : Fast, Slow.
- Partial Array Self-Refresh : 1/8, 1/4, 1/2, full

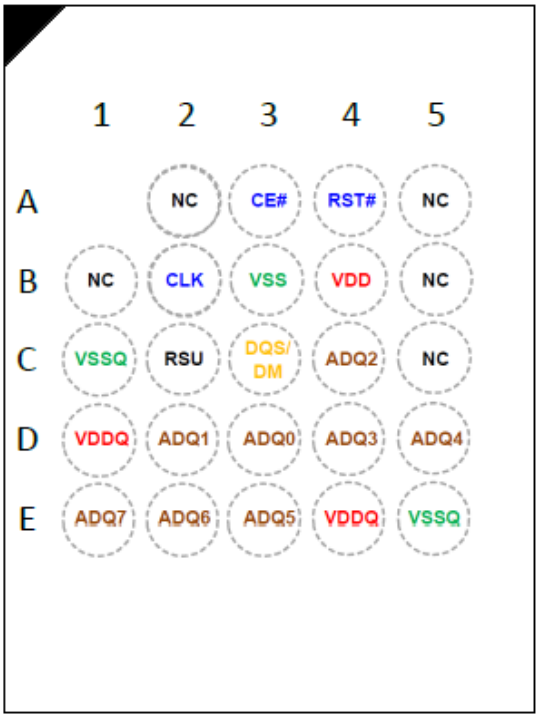
Order Information

Part No.	VDD/VDDQ	Max Clock	Temperature Range	Package
CS84641QA-5	1.62V~1.98V	200 MHz	-40°C to 85°C	24 balls BGA
CS84641QA-4		250 MHz		
CS84643QA-5	2.7V~3.6V	200 MHz		
CS84643QA-4		250 MHz		

Package Ballout and Addressing

24 ball TFBGA-6x8mm

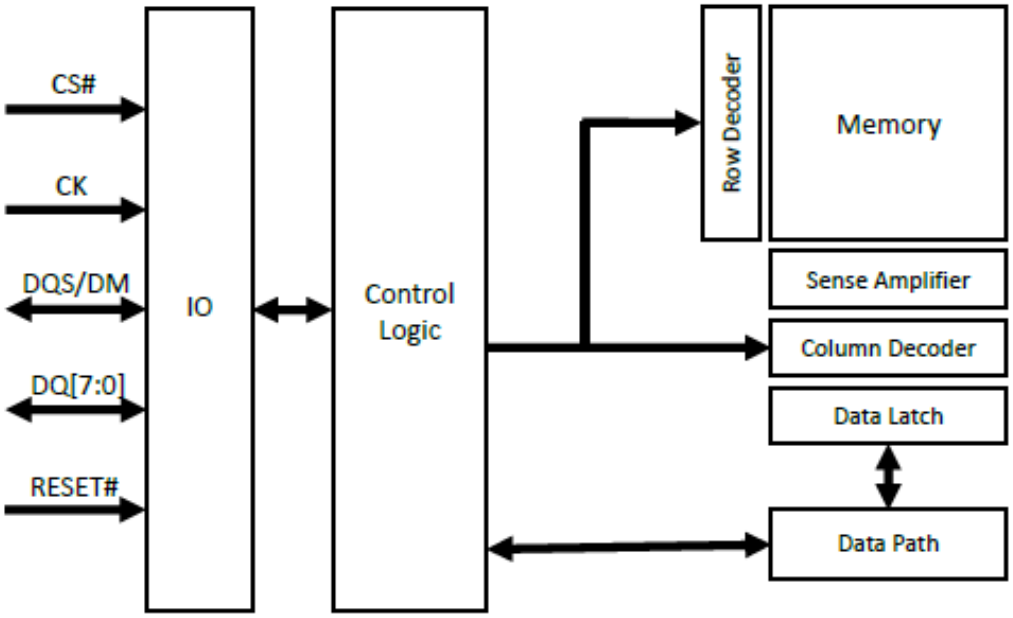
Top View



Pin Descriptions

Symbol	Type	Function
CE#	Input	Chip Select: CE# enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when CE# is sampled HIGH.
CLK	Input	Clock: CLK is driven by the system clock. All inputs to this device are acquired in synchronization with the rising and falling edge of this pin.
RST#	Input	Reset signal: Reset is active when RST# is sampled LOW. The RST# input includes a weak pull-up inside the device. If RST# is left unconnected, it will be pulled up to the HIGH state.
DQS/DM	I/O	Data Strobe & Date Mask: Output during read operation as Data Strobe (DQS) and Input during write operation as Data Mask (DM). Input data is masked when DM is sampled HIGH along with that input data during write operation.
A/DQ[7:0]	I/O	Data Input/Output: Command, Address, and Data information is transferred on these signals during read and write operation.
VDD	Power Supply	Power Supply
VDDQ	Power Supply	DQ Power Supply
VSS	Power Supply	Ground
VSSQ	Power Supply	DQ Ground

Logic Block Diagram



Note 1: This Logic Block Diagram is intended to facilitate user understanding of the operation of the device; it does not represent an actual circuit implementation.

Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. VDD and VDDQ must be applied simultaneously. When they reach a stable level at or above minimum VDD, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.
During Phase 1 CE# should remain HIGH (track VDD within 200mV); CLK should remain LOW.
After Phase 2 is complete the device is ready for operation.

Power-Up Initialization Method 1 (via. RESET# pin)

The RESET# pin can be used to initialize the device during Phase 2 as follow

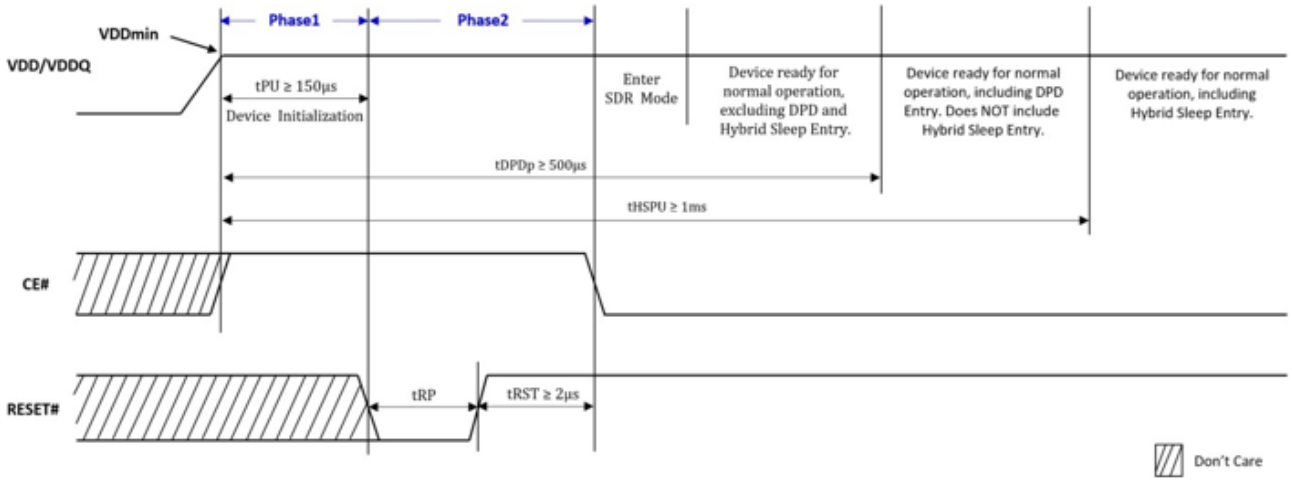


Figure 1. Power-Up Initialization Method 1 RESET#

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

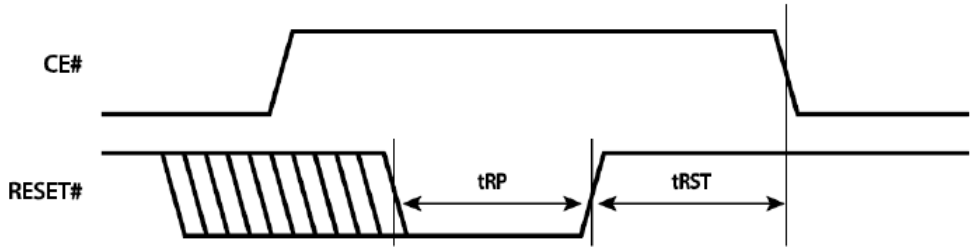


Figure 2. RESET# Timing

Power-Up Initialization Method 2(via. Global Reset)

As an alternate power-up initialization method, After the Phase 1 150µs period the Global Reset command is used to reset the device in Phase 2 as follows:

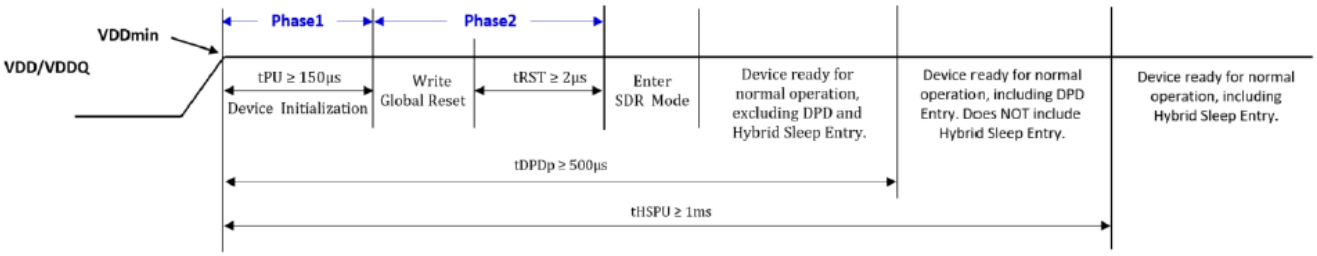


Figure 3. Power-Up Initialization Method 2 Timing with Global Reset

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below. Note that Global Reset command can be used ONLY as Power-up initialization.

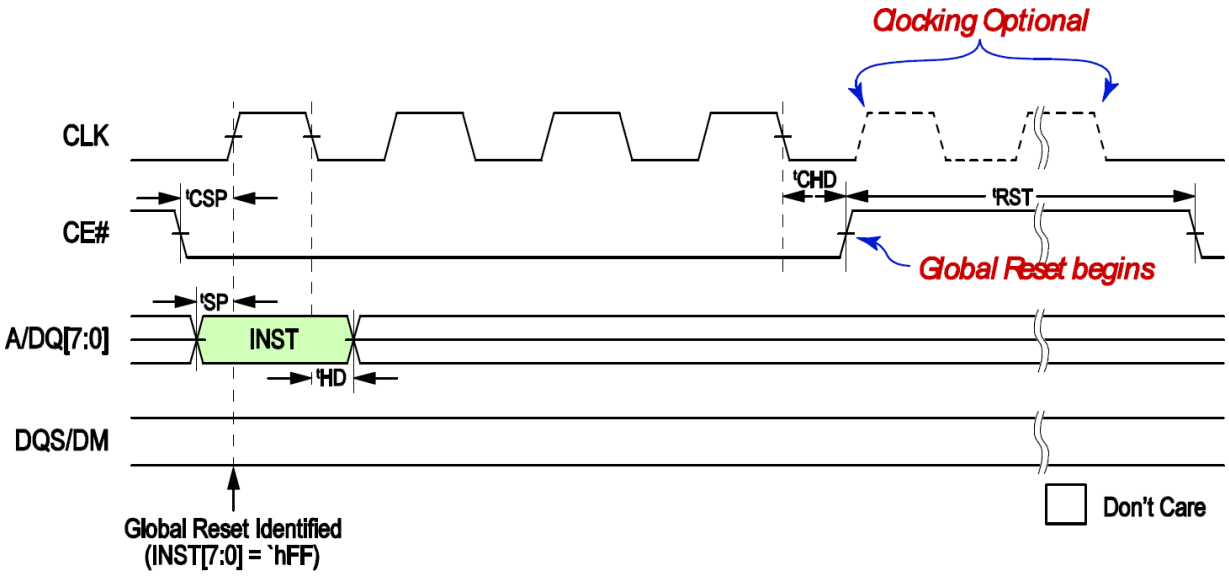


Figure 4. Global Reset

Interface Description

Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]='0). Mode Register accesses allow both even and odd addresses.

Burst Type and Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 1K bytes in standard or Hybrid wrap modes are register configurable (see Table 20). The device also includes command for Linear Bursting. Bursts can start on any even address. Write burst length has a minimum of 2 bytes.Read has no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

Command/Address Latching

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th,5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

Comment Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

Command	1st CLK		2nd CLK		3rd CLK	
	↑	↓	↑	↓	↑	↓
Sync Read	'h00		A3	A2	A1	A0
Sync Write	'h80		A3	A2	A1	A0
Sync Read (Linear Burst)	'h20		A3	A2	A1	A0
Sync Write (Linear Burst)	'hA0		A3	A2	A1	A0
Mode Register Read	'h40		X			MA
Mode Register Read	'hC0		X			MA
Global Reset	'hFF		X			

Remarks: A0 = CA[7:0]
A1 = RA[5:0], CA[9:8]
A2 = 1'bx, RA[12:6], unused address bit is reserved A3 = unused address bit is reserved
MA = Mode Register Address
X = don't care (V_{IH}/V_{IL})

Read Operation

After address latching, the device initializes DQS/DM to '0 from next CLK rising edge of the 3rd clock cycle (A1). See Figure 5 below. Output data is available after LC latency cycles, as shown in Figure 7 & Figure 8, LC is defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 30 & Table 31.
In case of internal refresh insertion, variable latency output data may be delayed by up to (LC*2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere between LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

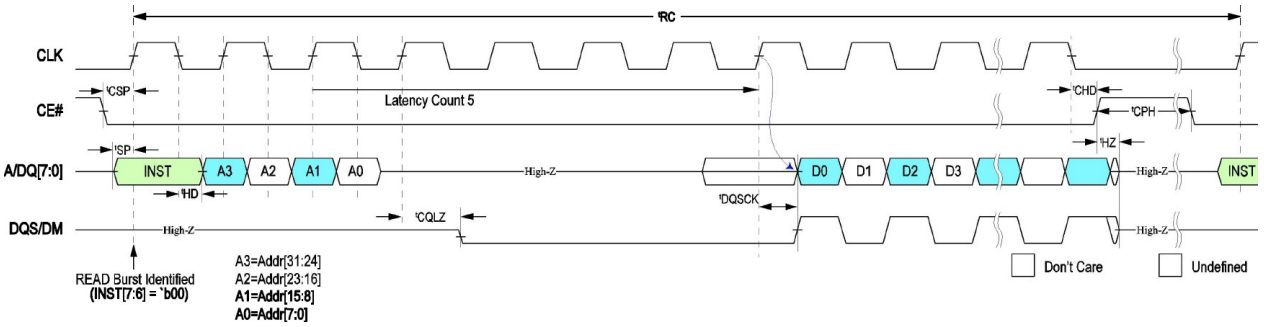


Figure 5: Synchronous Read

If RBX has been enabled (MR8[3] written to 1) and a Linear Burst Command issued, then Wrap settings (MR8[2:0] are ignored and Read operations are allowed to cross row boundaries as shown in Figure 6.

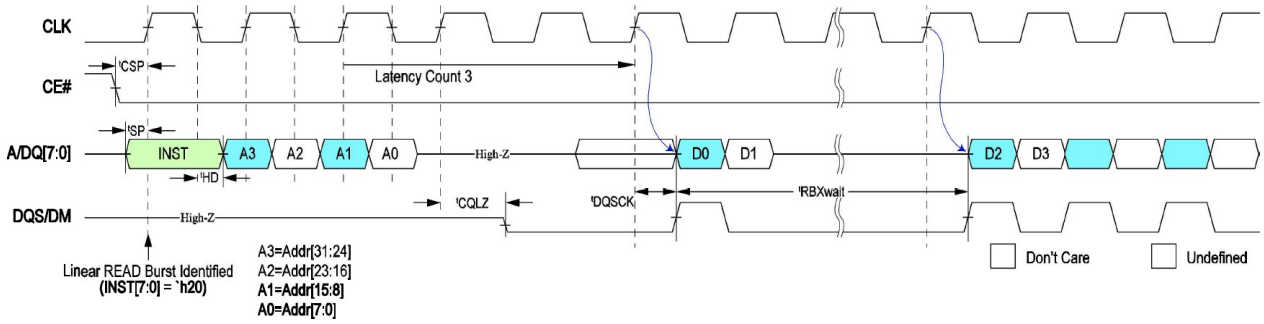


Figure 6: Synchronous Read with RBX (starting address '3FE)

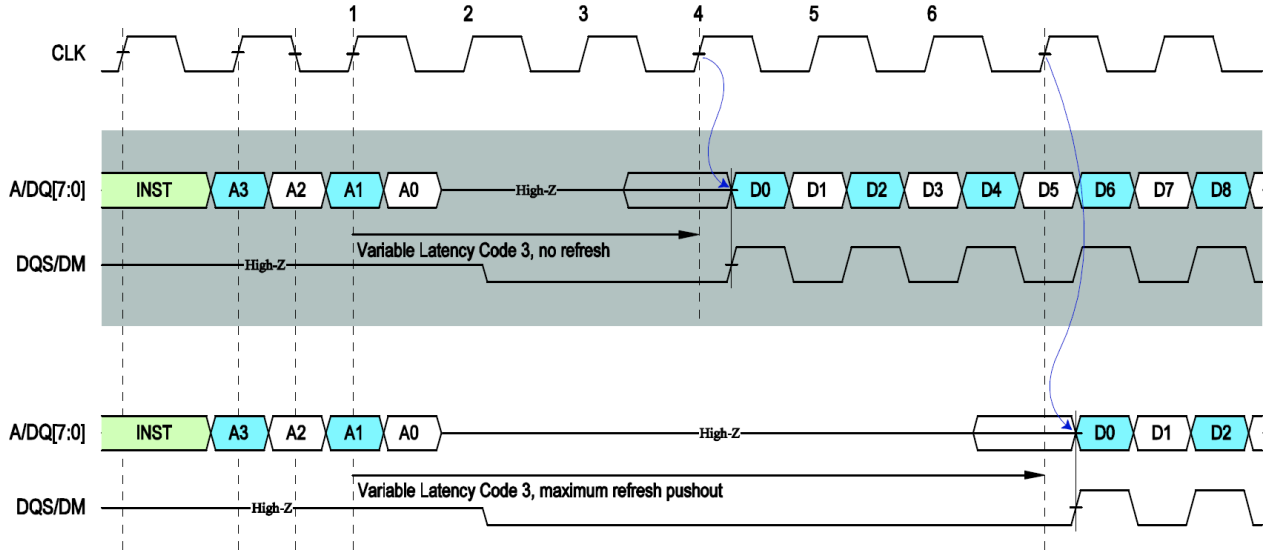


Figure 7: Variable Read Latency Refresh Pushout

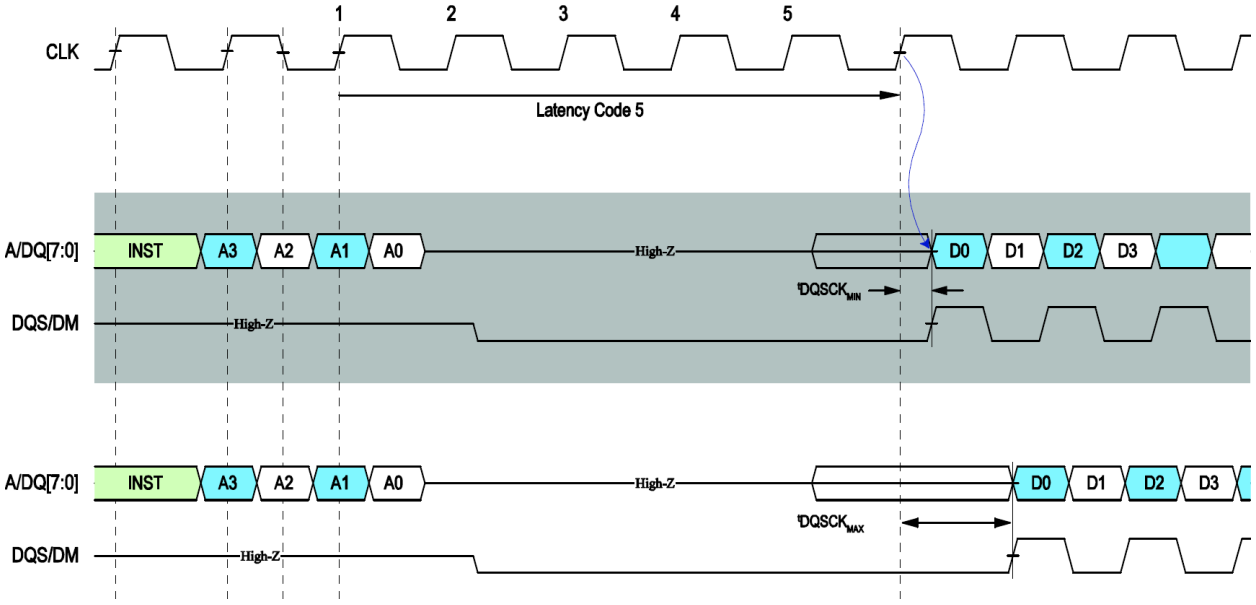


Figure 8: Read Latency & tDQSCK

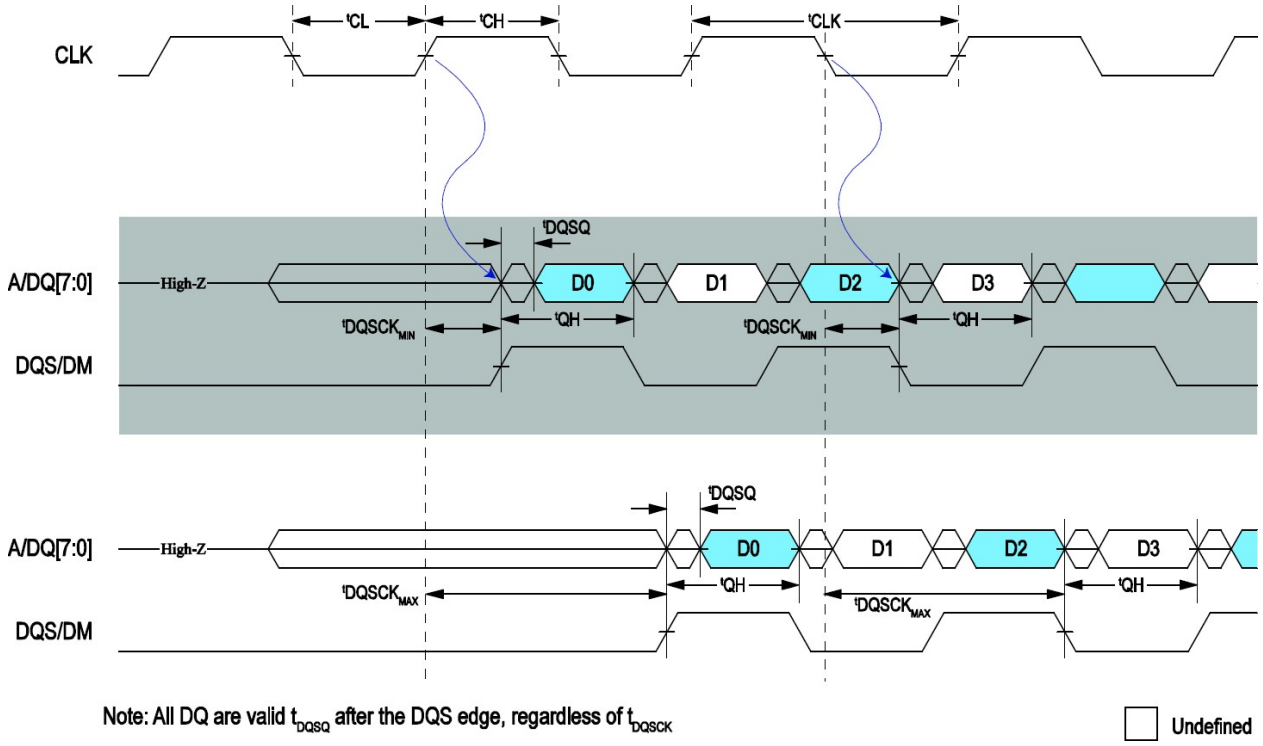


Figure 9: Read DQS/DM & DQ timing

Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 10.

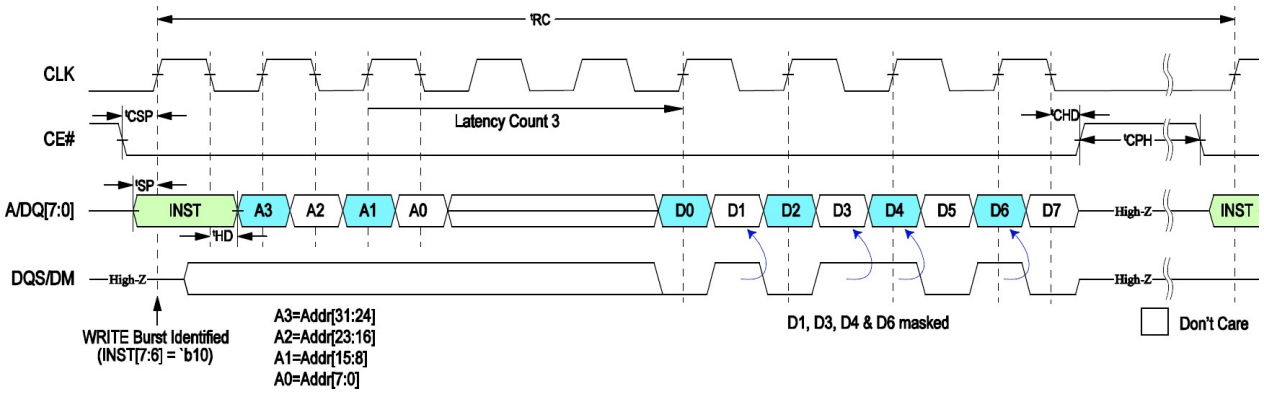


Figure 10: Synchronous Write followed by any operation

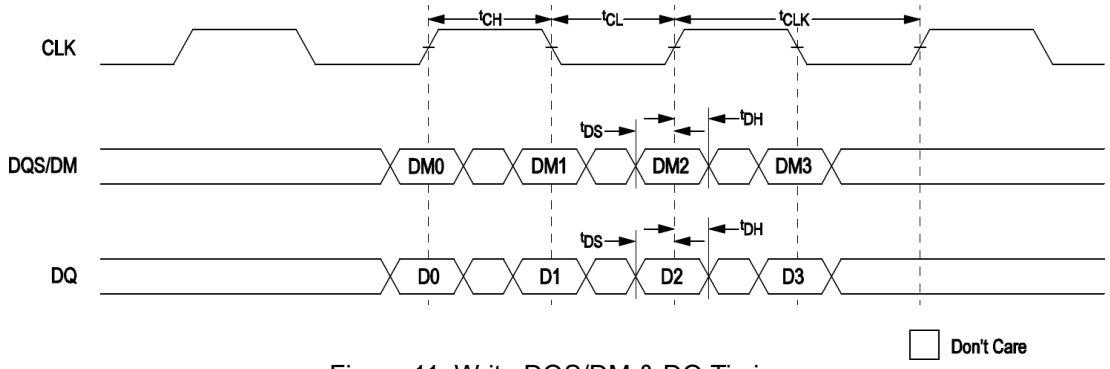
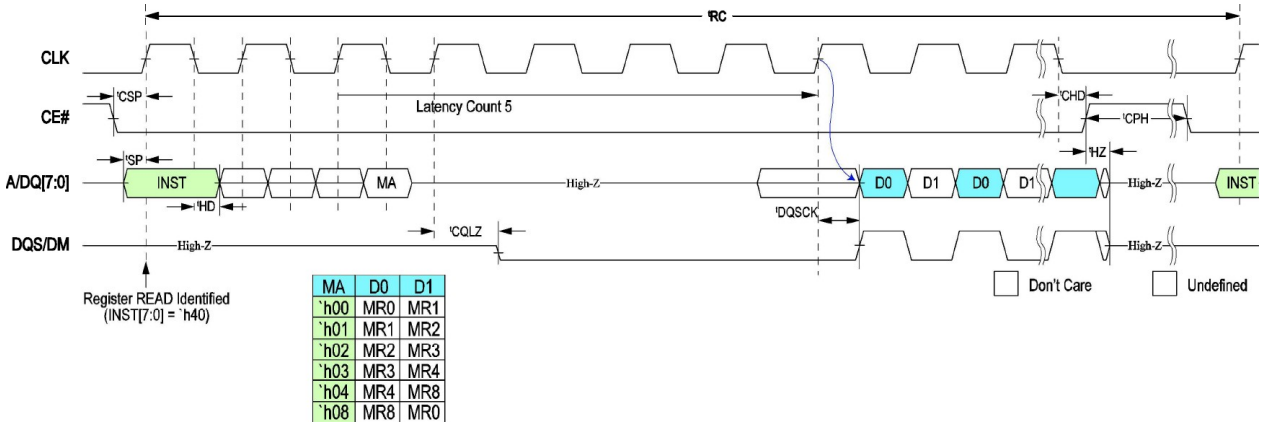


Figure 11: Write DQS/DM & DQ Timing

Control Registers

Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data 0 (see chart in the Figure below).



MA	D0	D1
`h00	MR0	MR1
`h01	MR1	MR2
`h02	MR2	MR3
`h03	MR3	MR4
`h04	MR4	MR8
`h08	MR8	MR0

Figure 12: Register Read

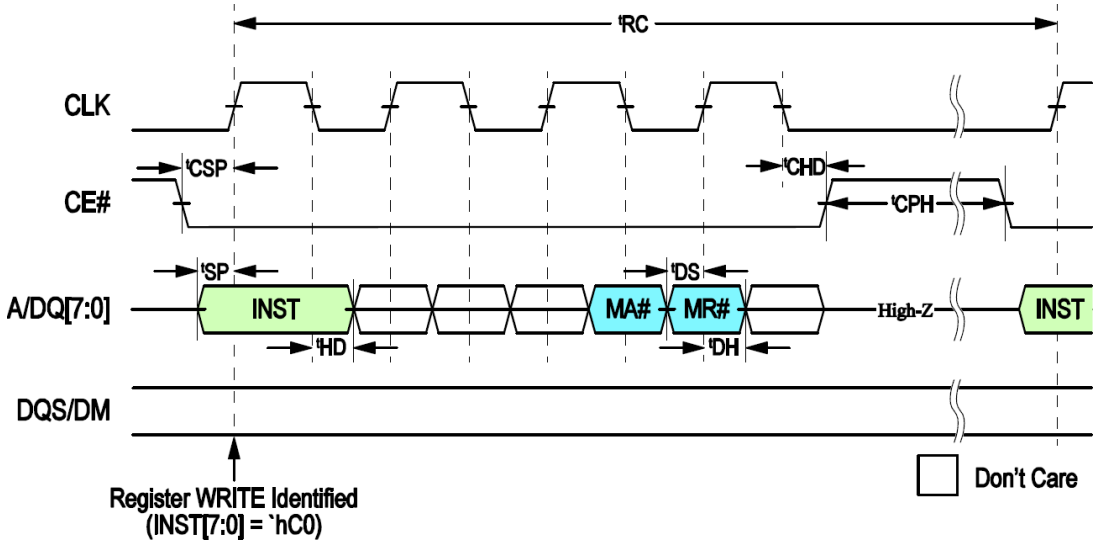


Figure 13: Register Write

Register Writes are Latency 1, whereas Register Reads use the same MR0[4:2] settings as burst reads (see Table 5). Registers 0, 4 & 8 are read and writable, and Registers 1, 2 and 3 are read-only. Register mapping is shown in Table 3. Note that MR0[6], MR0[7], MR4[4] and MR8[7] must be written to b'0.

Table 3: Mode Register Table

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	‘h00	R/W	‘00’		LT	Read Latency Code			Drive Str.	
1	‘h01	R	ULP	Rsvd.		Vendor ID				
2	‘h02	R	GB	Rsvd.		Dev ID		Density		
3	‘h03	R	RBXen	VDD	SRF	Rsvd.				
4	‘h04	R/W	Write Latency Code			‘0’	RF	PASR		
6	‘h06	W	Hybrid Sleep & DPD				Rsvd.			
8	‘h08	R/W	‘0’	Rsvd.			RBX	BT	BL	

Table 4: Read Latency Type (MR0[5])

Latency Type	
MR0[5]	LT
0	Variable (default)
1	Fixed

Table 5: Read Latency Codes MR0[5:2]

	VL Code (MR0[5]=0)		FL Code (MR0[5]=1)	Max Input CLK Freq (MHz)	
MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended
000	3	6	6	66	66
001	4	8	8	109	109
010	5 (Default)	10	10	133	133
011	6	12	12	166	166
100	7	14	14	200	200
101	8	16	16	200	200
110	9	18	18	250	250
Others	Reserved			-	-

Table 6: Operation Latency Code Table

Type	Operation	VL(default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

Table 7: Drive Strength Codes MR0[1:0]

Codes	Drive Strength	
	1.8V	3V
‘00	25Ω (Full)	50Ω (1/2)
‘01	50Ω (1/2 default)	100Ω (1/4 default)
‘10	100Ω (1/4)	200Ω (1/8)
‘11	200Ω (1/8)	400Ω (1/16)

Table 8: Ultra Low Power Device mapping MR1[7]

Codes	Ultra Low Power
‘0	Non Ultra Low Power (no Hybrid Sleep)
‘1	Ultra Low Power (Hybrid Sleep supported)

Table 9: Vendor ID mapping MR1[4:0]

Vendor ID
01110

Table 10: Good-Die Bit MR2[7]

Codes	Good Die ID
‘1	Pass
‘0	Fail

Table 11: Device ID MR2[4:3]

Codes	Good Die ID
‘00	Reserved
‘01	Reserved
‘10	Generation 3 (default)
Others	Reserved

Table 12: Device Density mapping MR2[2:0]

MR2[2:0]	Density
‘001	32Mb
‘011	64Mb
‘101	128Mb
‘111	256Mb
Others	Reserved

Table 13: Row Boundary Crossing Enable MR3[7]

MR3[7] (read only)	RBXen
‘0	RBX not supported
‘1	RBX supported via MR8[3]=1

Table 14: Operating Voltage Range MR3[6]

MR3[6]	VDD
‘0	1.8V
‘1	3V

Table 15: Self Refresh Flag MR3[5]

MR3[5] (read only)	Self Refresh Flag
‘0	Slow Refresh (allowed via MR4[3]=1, otherwise Fast Refresh
‘1	Fast Refresh

MR3[5] is a refresh indicator that corresponds to device internal temperature. This bit will indicate 0 when the temperature is low enough to allow a slow frequency refresh rate.

Table 16: Write Latency MR4[7:5]

MR4[7:5]	Write Latency	Fmax (MHz)
‘000	3	66
‘100	4	104
‘010	5	133
‘110	6	166
‘001	7	200
‘101	8	200
‘011	9	250
Others	Reserved	-

Table 17: Refresh Frequency MR4[3]

MR4[3]	Refresh Frequency
‘0	Fast Refresh
‘1	Enable Slow Refresh when temperature allows

The Partial Array Self-Refresh (PASR) bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

Table 18: Partial Array Self-Refresh MR4[2:0]

64Mb				
Codes	**Refresh Coverage**	**Address Space**	**Size**	**Density**
‘000	Full array (default)	000000h~7FFFFFh	8M x8	64Mb
‘001	Bottom 1/2 array	000000h~3FFFFFh	4M x8	32Mb
‘010	Bottom 1/4 array	000000h~1FFFFFh	2M x8	16Mb
‘011	Bottom 1/8 array	000000h~0FFFFFh	1M x8	8Mb
‘100	None	0	0M	0Mb
‘101	Top 1/2 array	400000h~7FFFFFh	4M x8	32Mb
‘110	Top 1/4 array	600000h~7FFFFFh	2M x8	16Mb
‘111	Top 1/8 array	700000h~7FFFFFh	1M x8	8Mb

Table 19: Ultra Low Power Modes MR6[7:0]

MR6[7:0]	Ultra Low Power Modes
‘hF0	Hybrid Sleep
‘hC0	Deep Power Down
Others	Reserved

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (1K) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 1K lengths.

Table 20: Burst Type MR8[2], Burst Length MR8[1:0]

MR8[2]	***MR8[1:0]***	***Burst Length***	***Example of Sequence of Bytes During Wrap***	
			Starting Address	***Byte Sequence***
‘0	‘00	16 Byte Wrap	4	[4,5,6,…15,0,1,2,…]
‘0	‘01	32 Byte Wrap	4	[4,5,6,…31,0,1,2,…]
‘0	‘10	64 Byte Wrap	4	[4,5,6,…63,0,1,2,…]
‘0	‘11	1K Byte Wrap	4	[4,5,6,…1023,0,1,2,…]
‘1	‘00	16 Byte Hybrid Wrap	2	[2,3,4,…15,0,1],16,17,18,…1023,0,1,…
‘1	‘01	32 Byte Hybrid Wrap (default)	2	[2,3,4,…31,0,1],32,33,34,…1023,0,1,…
‘1	‘10	64 Byte Hybrid Wrap	2	[2,3,4,…63,0,1],64,65,66,…1023,0,1,…
‘1	‘11	1K Byte Wrap	2	[2,3,4,…1023,0,1,2,…]

The Linear Burst Commands (INST[5:0]=6’b100000) override MR8[2:0] settings and forces the current array read or write command to do 1K Byte Wrap (equivalent to having MR8[1:0] set to 2’b11). The burst continues linearly from the starting address and at the end of the page, then wraps back to the beginning of the page. This special burst instruction can be used on both array write and read.

Table 21: Row Boundary Crossing Read Enable MR8[3]

MR8[3]	RBX Read
‘0	Reads stay within the 1K column address space
‘1	Reads cross row at 1K boundaries

This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within the 1K (CA=’h000 -> ‘h3FF) column address space. Setting this bit high will allow Linear Burst reads to cross over into the next Row (RA+1).

Hybrid Sleep Mode

When the PSRAM is not needed for system operation but data in the device needs to be retained, it may be placed in Hybrid Sleep Mode to save more power. Hybrid Sleep Mode Entry is entered by writing 8‘hF0 into MR6. CE# going high initiates the Hybrid Sleep mode and must be maintained for the minimum duration of tHS. The Hybrid Sleep Entry command sequence is shown below.

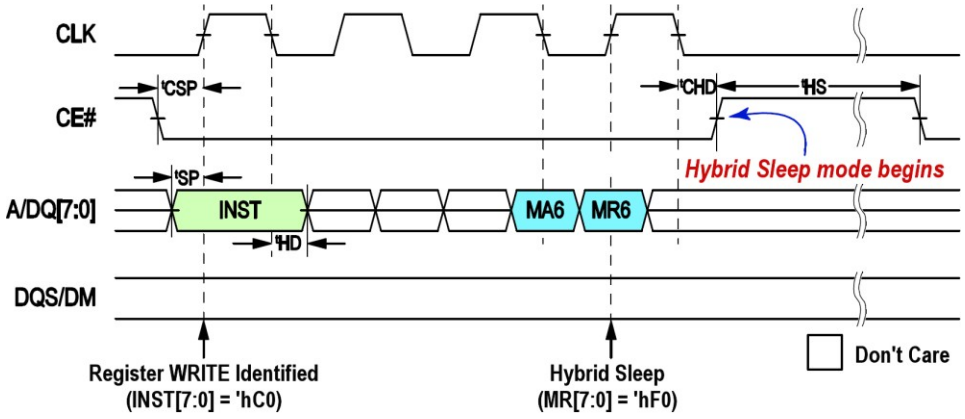


Figure 14: Hybrid Sleep Entry Write (default WL0)

Hybrid Sleep Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

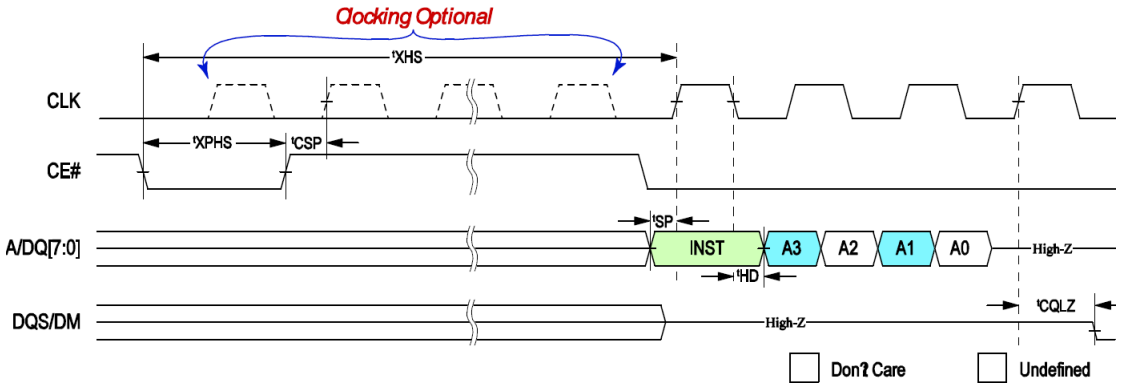


Figure 15: Hybrid Sleep Exit (Read Operation shown as example)

Deep Power Down Mode

Deep Power Down Mode (DPD) is a feature which puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.

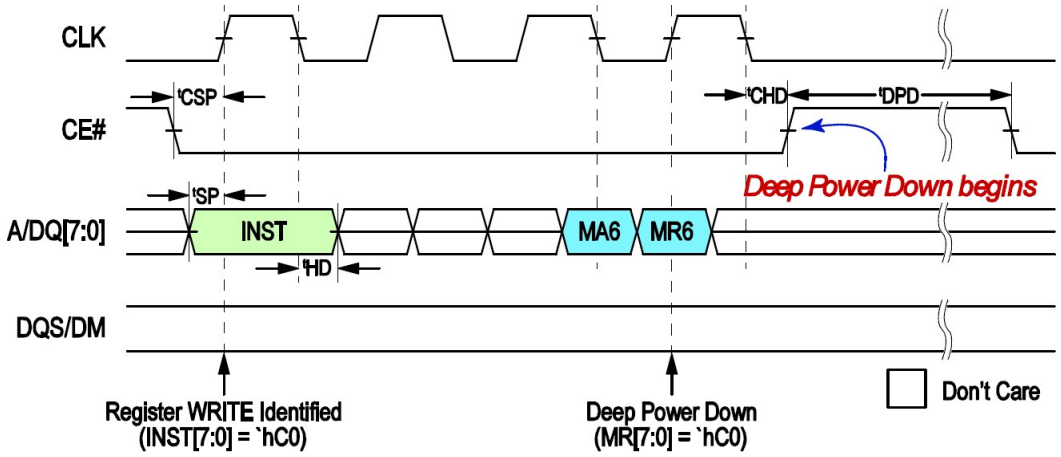


Figure 16: Deep Power Down Entry

Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD Exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum tXDPD).

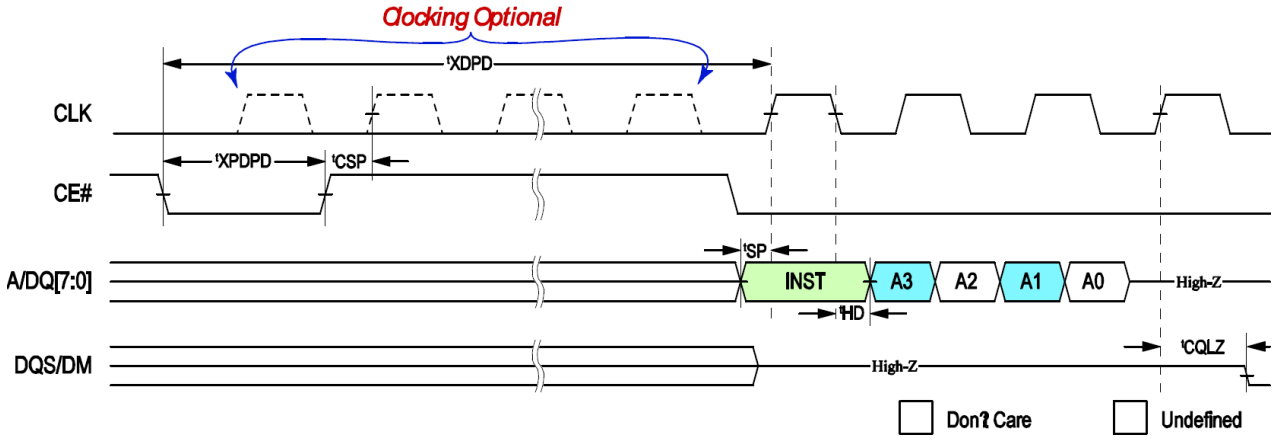


Figure 17: Deep Power Down Exit (Read Operation shown as example)

Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial power up to the first DPD entry.

Electrical Specification

Absolute Maximum Ratings

Table 22: Absolute Maximum Ratings

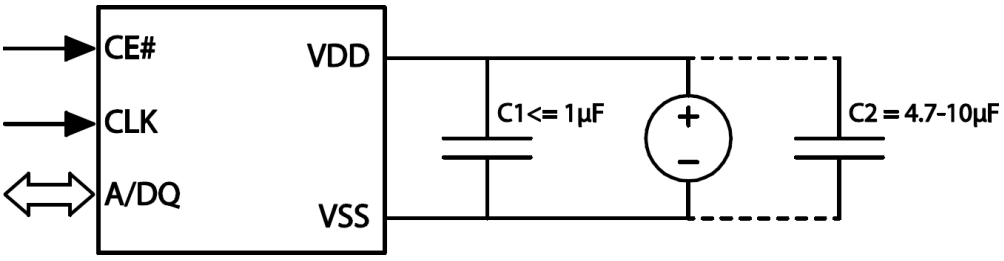
Parameter	Symbol	Rating	Unit
Voltage to any ball except VDD, VDDQ relative to VSS	VT	-0.4 to VDD/VDDQ+0.4	V
Voltage on VDD supply relative to VSS	VDD	-0.4 to +2.45	V
Voltage on VDDQ supply relative to VSS	VDDQ	-0.4 to +2.45	V
Storage Temperature	TSTG	-55 to +150	°C

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



Low ESR cap C1

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

Large cap C2

During hybrid sleep modes even though hybrid sleep average currents are very small (less than 100µA), device will internally have low duty cycle burst refresh for an extended period of time of a few tens of microseconds. These refresh current peaks are large. During this period if the system regulator cannot supply large peaks for several microseconds, it is important to place a 4.7µF-10µF cap to take care of burst refresh currents and replenish the charge before next burst of refreshes.

DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{DD}	Supply voltage	1.62	1.98	V	
V_{DDQ}	DQ supply voltage	1.62	1.98	V	
V_{IH}	Input high leakage	V_{DDQ}-0.4	V_{DDQ}+0.2	V	
V_{IL}	Input low leakage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DDQ}		V	
V_{OL}	Output high voltage (I_{OL}=+0.2mA)		0.2 V_{DDQ}	V	
I_{LI}	Input leakage current		1	μA	
I_{LO}	Output leakage current		1	μA	
ICC	Read/Write @13MHz		4	mA	
	Read/Write @133MHz		16	mA	
	Read/Write @200MHz		22	mA	
ISB_{STD}	Standby current (85°C) @ 1.8V		200	μA	
ISB_{EXT}	Standby current (105°C) @ 1.8V				
ISB_{STDDPD}	Standby current (Deep power down)		15	μA	

ISB Partial Array Refresh Current

Typical PASR Current @ 1.8V, 25°C

Standby Current @ 25 °C			
PASR	**ISB-typical mean**	**Uint**	**Note**
Full	66	μA	
1/2		μA	
1/4		μA	
1/8		μA	
Hybrid Sleep Current @ 25 °C			
PASR	**ISB-typical mean**	**Uint**	**Note**
Full	20	μA	
1/2		μA	
1/4		μA	
1/8		μA	

Typical PASR Current @ 1.8V, 85°C

Standby Current @ 85 °C			
PASR	**ISB-typical mean**	**Uint**	**Note**
Full	190	μA	
1/2		μA	
1/4		μA	
1/8		μA	
Hybrid Sleep Current @ 85 °C			
PASR	**ISB-typical mean**	**Uint**	**Note**
Full	120	μA	
1/2		μA	
1/4		μA	
1/8		μA	

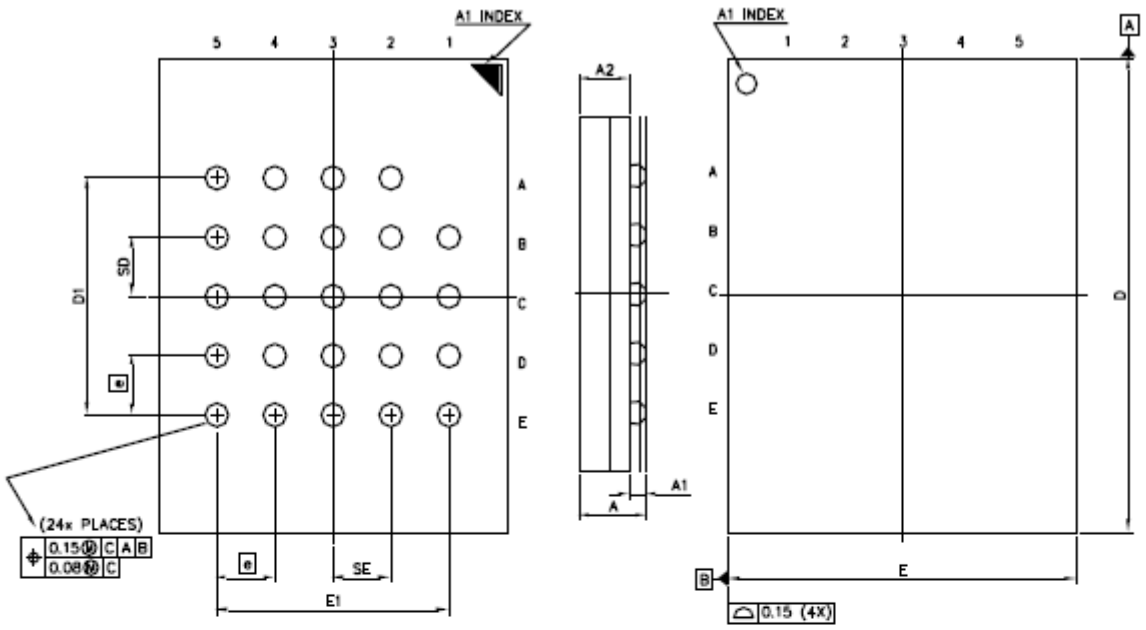
AC Characteristics

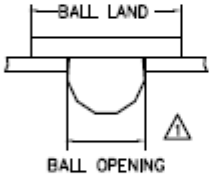
Symbol	Parameter		133MHz		166MHz		200MHz		250MHz		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
tCK	Clock cycle time		7.5	-	6	-	5	-	4	-	ns
tCH/tCL	Clock high/low width		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
tKHKL	CLK rise or fall time		-	1.2	-	1	-	0.8	-	0.8	ns
tCPH	CE# HIGH between subsequent burst operations		15	-	18	-	20	-	28	-	ns
tCEM	CE# low pulse width	-40~85°C	-	8	-	8	-	8	-	8	μs
		85~105°C	-	3	-	3	-	3	-	3	μs
			3	-	3	-	3	-	3	-	tCK
tXPHS	HybridSleep Exit CE# low pulse width		-	tCEM	-	tCEM	-	tCEM	-	tCEM	μs
			60	-	60	-	60	-	60	-	ns
tCSP	CE# setup time to CLK rising edge		2	-	2	-	2	-	2	-	ns
tCSP2	CE# rising edge to next CLK falling edge		1.5	-	1.5	-	1.5	-	1.5	-	ns
tCHD	CE# hold time from CLK falling edge		2	-	2	-	2	-	2	-	ns
tSP	Setup time to active CLK edge		0.8	-	0.8	-	0.8	-	0.8	-	ns
tHD	Hold time from active CLK edge		0.8	-	0.8	-	0.8	-	0.8	-	ns
			-	0.75	-	0.75	-	0.75	-	0.75	tCK
tHZ	Chip disable to DQ/DQS output high-Z		-	6	-	6	-	6	-	6	ns
tRBXwait	Row Boundary Crossing Wait Time		30	65	30	65	30	65	30	65	ns
tRC	Write/Read Cycle		60	-	60	-	60	-	60	-	ns
tHS	Minimum Hybrid Sleep duration		150	-	150	-	150	-	150	-	μs

tXHS	Hybrid Sleep Exit CE# low to CLK setup time	150	-	150	-	150	-	150	-	µs
tDPD	Minimum DPD duration	500	-	500	-	500	-	500	-	µs
tDPDp	Minimum period between DPD	500		500		500		500		µs
tXDPD	DPD CE# low to CLK setup time	150	-	150	-	150	-	150	-	µs
tXPDPD	DPD Exit CE# low pulse width	60	-	60	-	60	-	60	-	ns
tPU	Device Initialization	150	-	150	-	150	-	150	-	µs
tRP	RESET# low pulse width	1	-	1	-	1	-	1	-	µs
tRST	Reset to CMD valid	2	-	2	-	2	-	2	-	µs
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	1	6	ns
tDQSCK	DQS output access time from CLK	2	5.5	2	5.5	2	5.5	2	5.5	ns
tDQSQ	DQS – DQ skew	-	0.6	-	0.5	-	0.4	-		ns
tDS	DQ and DM input setup time	0.8	-	0.8	-	0.8	-	0.8	-	ns
tDH	DQ and DM input hold time	0.8	-	0.8	-	0.8	-	0.8	-	ns

Package Outline

24 ball TFBGA-6x8 mm





Note:

Ball land: 0.45mm. Ball Opening: 0.35mm

PCB ball land suggested <= 0.35mm

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	---	---	1.20	---	---	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	---	0.85	---	---	0.033	---
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		